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Residential German Solar PV Inverter Test Report

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1.0 EXECUTIVE SUMMARY

This report will provide the dynamic performance of residential solar PV inverters designed to operate according to German grid code standards. The incentive for testing German grid code inverters is to evaluate the advanced features (voltage ride through, power curtailment, ramp rate, watts/over-frequency, voltage support, and communications) not currently available for inverters that follow U.S. standards. The following steady-state, transient, and harmonic test results will be used to support SCE Field Engineering's assessment of advanced inverter characteristics and uncover any potential negative impacts. As with the previous testing, the data will also be used to:

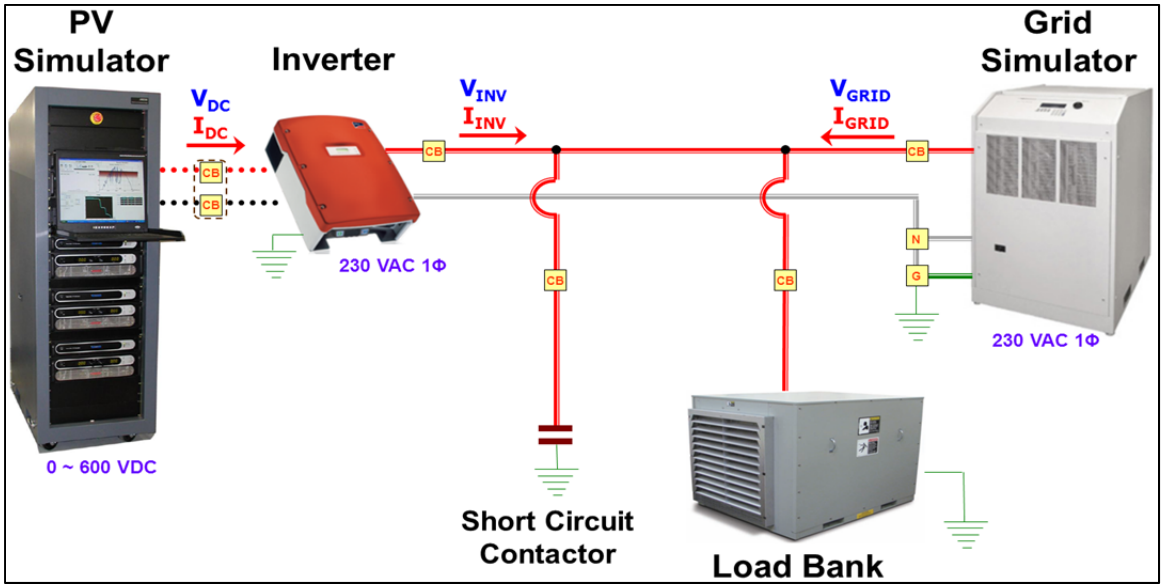
- Influence the standards revisions such as UL1741, IEEE 1547, and California Rule 21, in order to ensure that these devices support the reliability of the grid
- Develop and validate solar PV models for distribution system impact studies
- Review and revise, if necessary, SCE internal standards (interconnection or working practices)

Table 1.0.1 has the specifications of the tested inverters, all from a single manufacturer. All testing was performed using a nominal frequency of 60 Hz. Notice that inverters 202 and 204 are identical devices, and therefore to avoid redundant testing, inverter 204 was not tested. These inverters were tested in the Distributed Energy Resources (DER) Lab at SCE's Fenwick facility in Westminster, California.

Inverter #	Ratings						Topology
	$V_{AC\ (L\text{-}N)}$	Φ	$P_{GEN\ (kW)}$	Freq. (Hz)	PF	$V_{DC\ (MPPT)}$	
201	230	1	7.0	50 - 60	± 0.8	335 - 560	Transformer-based
202	230	1	5.0	50 - 60	± 0.8	246 - 480	Transformer-based
203	230	1	11.0	50 - 60	± 0.8	333 - 500	Transformerless
204	230	1	5.0	50 - 60	± 0.8	246 - 480	Transformer-based
205	230	1	4.6	50 - 60	± 0.8	175 - 500	Transformerless

Table 1.0.1 German Residential Solar PV Inverters Tested in Southern California Edison

0 shows the test setup used in this testing. A test procedure for this purpose was created and has been shared to other including manufactures, national laboratories, and other utilities.



TEST LAYOUT

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2.0 GRID DISCONNECTION TEST

The inverters were islanded with varying amounts of load to better understand the transient over-voltages (TOV) generated when disconnecting from the grid. Table 2.0.1 summarizes the different inverters behavior during islanding conditions.

Key findings:

- Transient over-voltages are highest when inverter is islanded with NO load (over-voltages can be reduced by increasing the load)
- All inverters also exhibit capacitor discharge behavior when disconnected with no load
- Only Inverter 202 falls outside the CBEMA curve, into the prohibited region, when islanded with no load
- The dynamic behavior is repeatable on all the inverters

Manuf. #	Inverter #	Rating (kW)	Load (kW)	% Load	$V_{MAXIMUM-INSTANTANEOUS}$ (%)	$t_{MAXIMUM}$ (cycles) for V > 100%	$t_{MAXIMUM}$ (cycles) for V > 10%
4	201	7	0.00	0%	145	0.7	7.6
			1.40	20%	133	0.5	0.7
			3.47	50%	122	0.5	0.7
			5.55	79%	116	4.9	5.6
			6.89	98%	103	4.3	5.1
	202	5	0.00	0%	195	1.0	7.8
			1.38	28%	172	0.4	0.5
			2.77	55%	147	0.5	0.6
			3.81	76%	126	0.5	0.6
			5.08	102%	101	0.0	5.6
	203	11	0.00	0%	164	2.8	116.3
			2.79	25%	141	0.4	0.6
			5.58	51%	132	0.5	0.6
			8.32	76%	126	0.1	0.4
			11.00	100%	101	0.0	5.2
	205	4.6	0.00	0%	147	3.0	19.4
			1.39	30%	129	0.5	0.6
			2.09	45%	126	0.5	0.5
			3.48	76%	122	9.3	10.0
			4.31	94%	109	4.7	8.2

Table 2.0.1 Inverters TOV

2.1 Inverter #201

Figure 2.1.1 and Figure 2.1.2 below shows Inverter 201 behavior when islanded with different amounts of load. Each test was performed several times as shown in the plots.

The key findings for this inverter are:

- Highest temporary overvoltage is 145% of nominal voltage and occurs when islanding with no load
- The maximum time when the voltage goes above 100% is less than 5 cycles
- Trips off within 8 cycles (within IEEE 1547 standard anti-islanding protection of 2 seconds)
- Negligible voltage discharge behavior when disconnected with no load
- Inverter 201 TOV falls within the CBEMA curve when disconnected with and without load

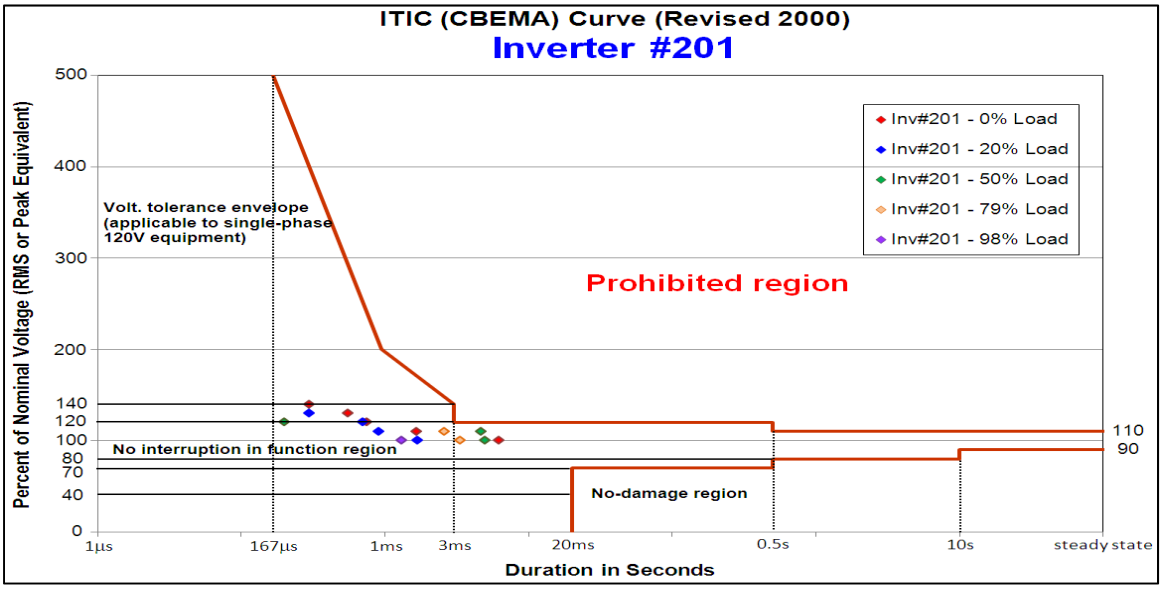

Figure 2.1.1 Inverter#201 TOV on ITIC (CBEMA)

The island of each test begins at the point where the voltage deviates from the normal steady state sinusoidal voltage waveform.

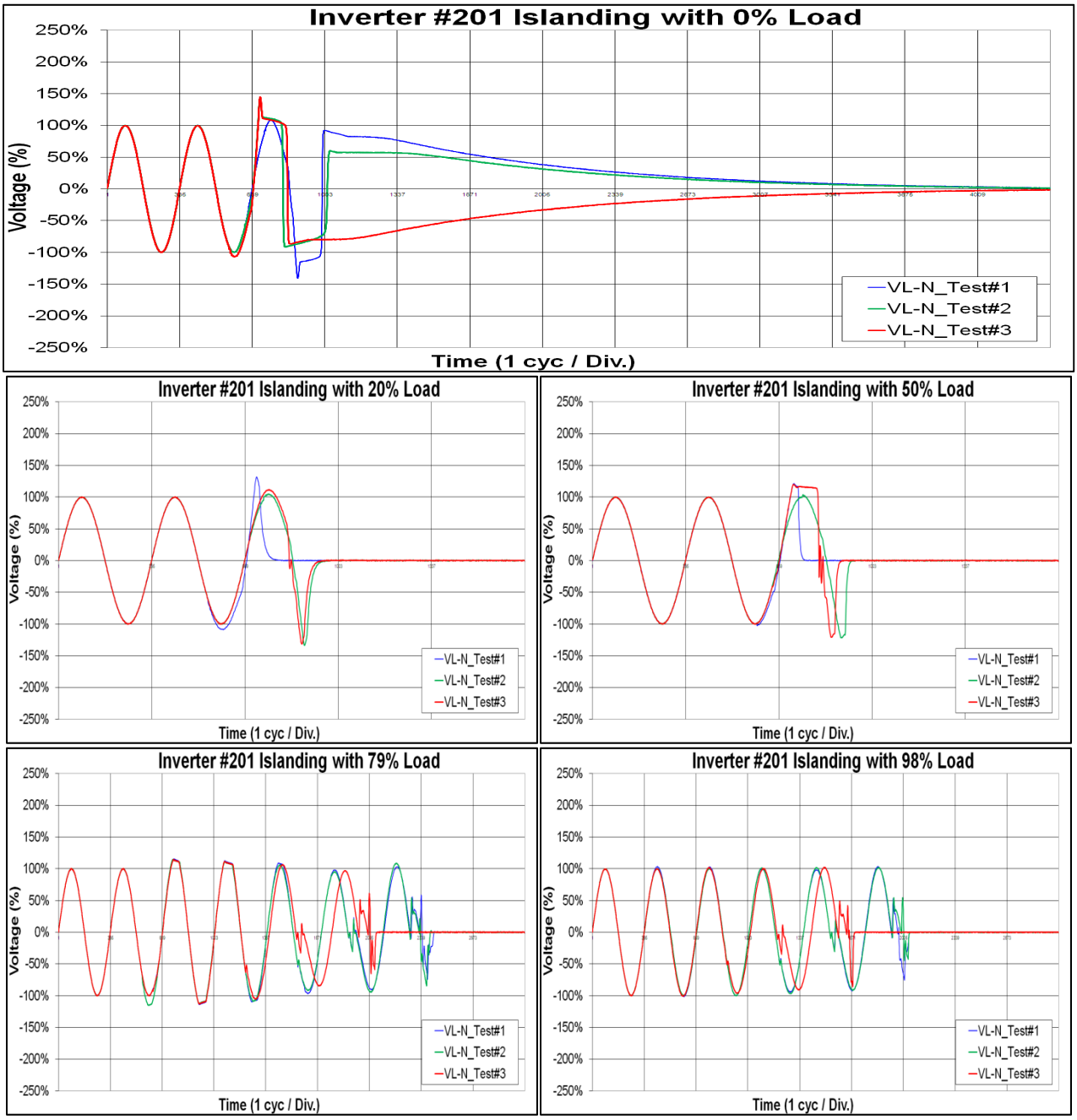

Figure 2.1.2 TOV During Grid Disconnection with Different Loads (Inverter #201)

2.2 Inverter #202

Figure 2.2.1 and Figure 2.2.2 shows Inverter 202 behavior when islanded with different amounts of load. Each test was performed several times as shown in the plots.

The key findings for this inverter are:

- Highest temporary overvoltage is 195% of nominal voltage and occurs when islanding with no load
- The maximum time when the voltage goes above 100% is less than 1 cycles
- Trips off within 8 cycles (within IEEE 1547 standard anti-islanding protection of 2 seconds)
- Negligible voltage discharge behavior when disconnected with no load
- Inverter 202 TOV falls outside the CBEMA curve when disconnected with no load

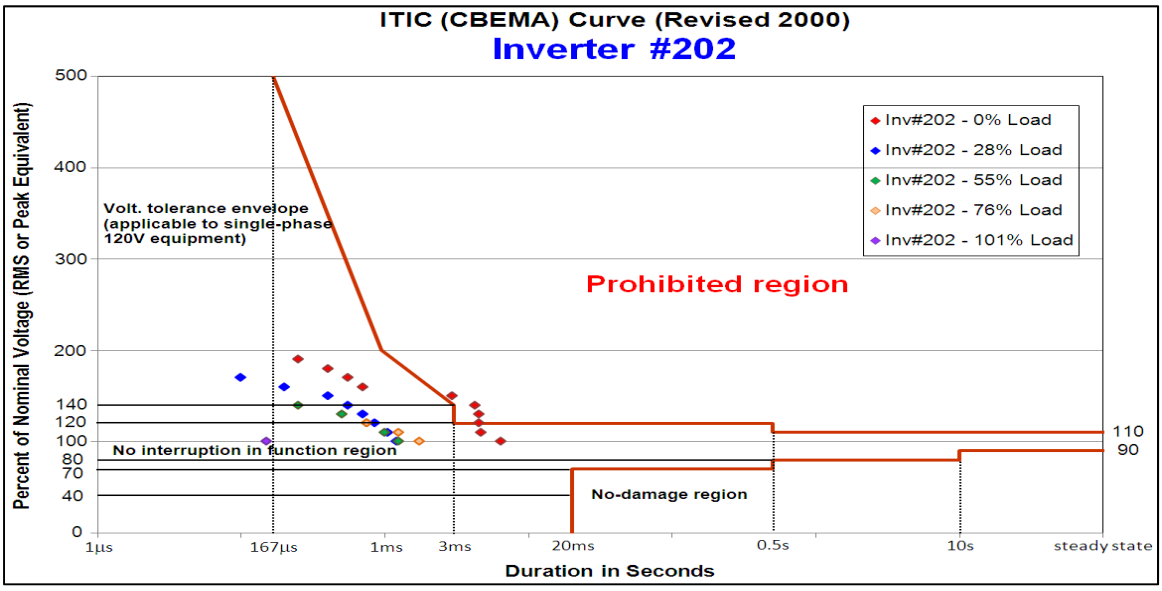

Figure 2.2.1 Inverter#202 TOV on ITIC (CBEMA)

The island of each test begins at the point where the voltage deviates from the normal steady state sinusoidal voltage waveform.

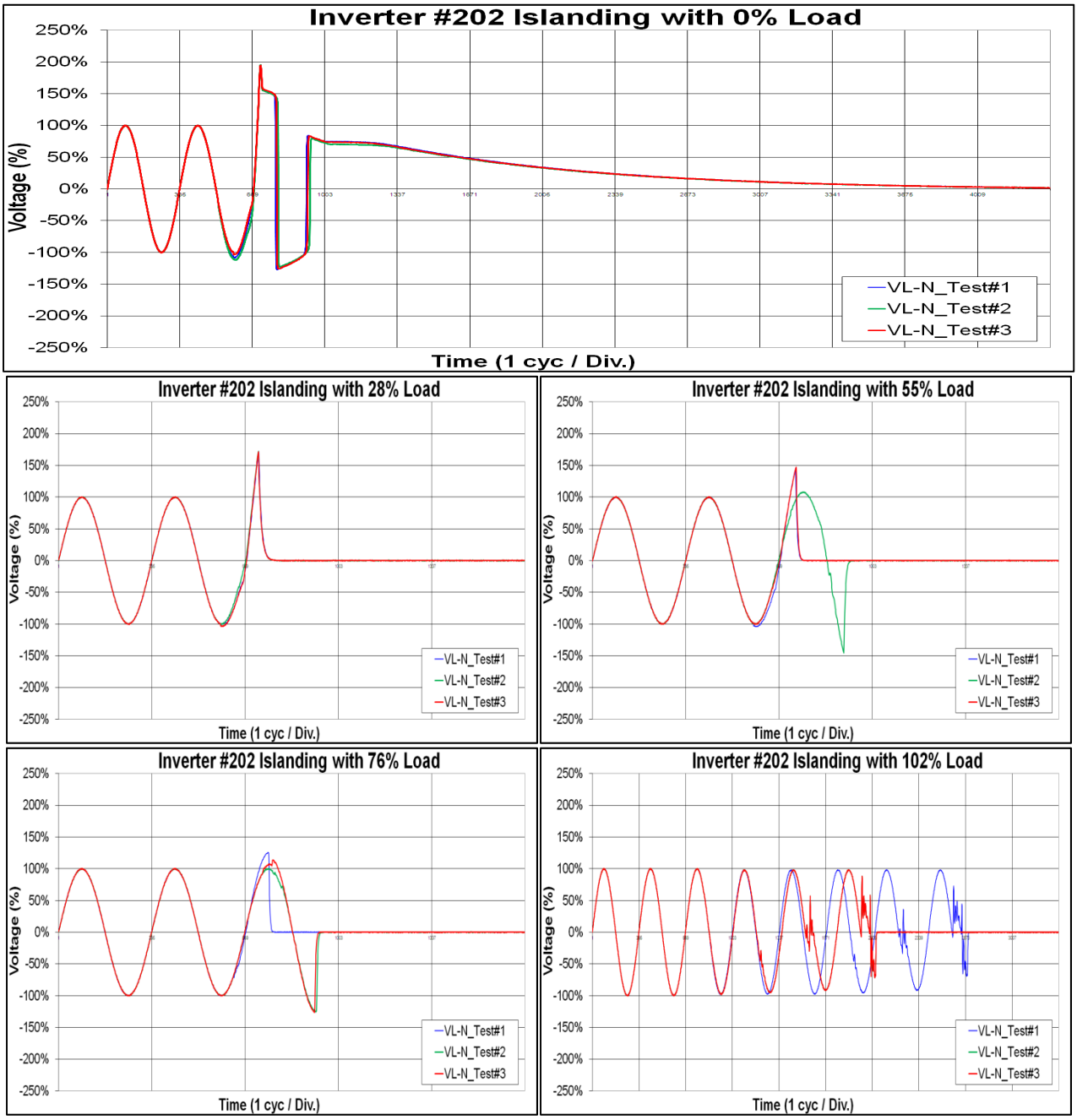

Figure 2.2.2 TOV During Grid Disconnection with Different Loads (Inverter #202)

2.3 Inverter #203

Figure 2.3.1 and Figure 2.3.2 below indicate the behavior for Inverter 203 when islanded with different amounts of load. Each test was performed several times as shown in the plots.

The key findings for this inverter are:

- Highest temporary overvoltage is 164% of nominal voltage and occurs when islanding with no load
- The maximum time when the voltage goes above 100% is less than 3 cycles
- Trips off within 117 cycles (within IEEE 1547 standard anti-islanding protection of 2 seconds)
- Longest voltage discharge behavior of all German inverters when disconnected with no load
- Inverter 203 TOV falls within the CBEMA curve when disconnected with and without load

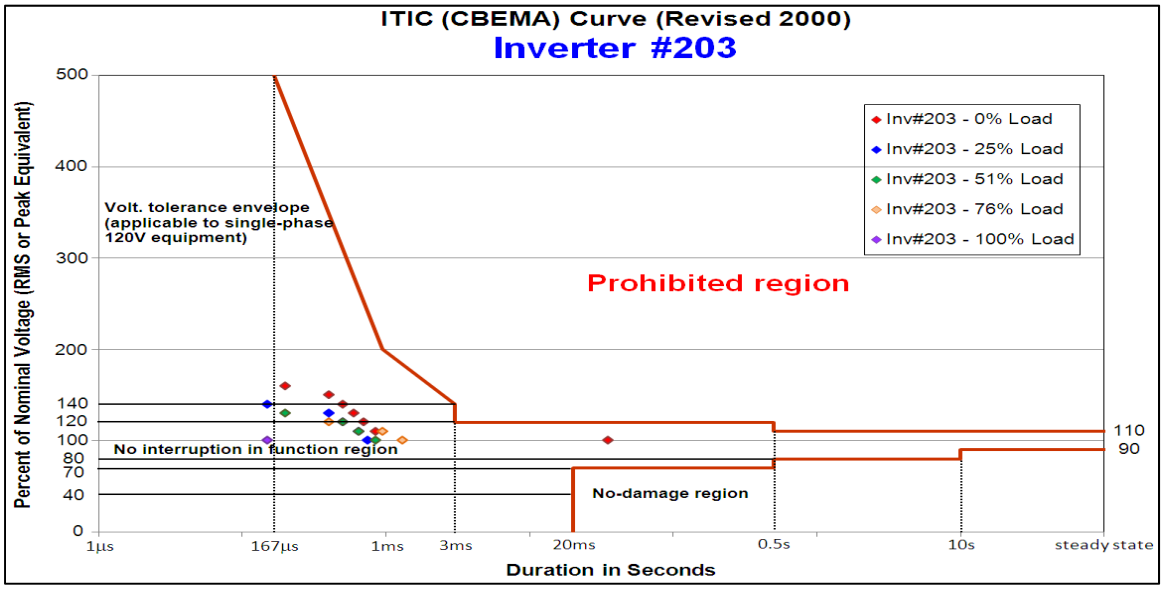

Figure 2.3.1 Inverter#203 TOV on ITIC (CBEMA)

The island of each test begins at the point where the voltage deviates from the normal steady state sinusoidal voltage waveform.

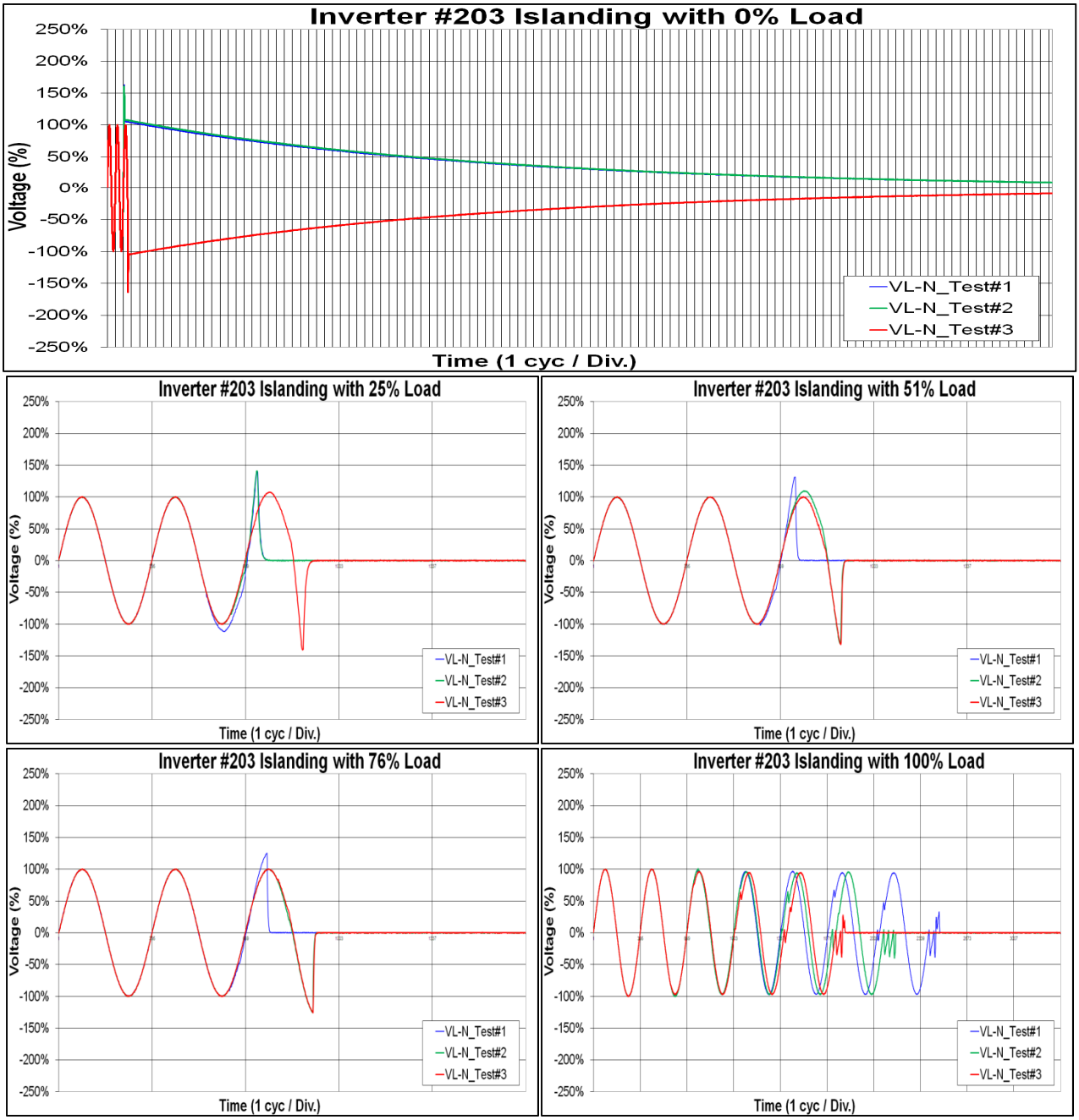

Figure 2.3.2 TOV During Grid Disconnection with Different Loads (Inverter #203)

2.4 Inverter #205

Figure 2.4.1 and Figure 2.4.2 below shows Inverter 205 behavior when islanded with different amounts of load. Each test was performed several times as shown in the plots.

The key findings for this inverter are:

- Highest temporary overvoltage is 147% of nominal voltage and occurs when islanding with no load
- The maximum time when the voltage goes above 100% is less than 9.3 cycles (at 76% rated load)
- Trips off within 20 cycles (within IEEE 1547 standard anti-islanding protection of 2 seconds)
- Negligible voltage discharge behavior when disconnected with no load
- Inverter 205 TOV falls within the CBEMA curve when disconnected with and without load

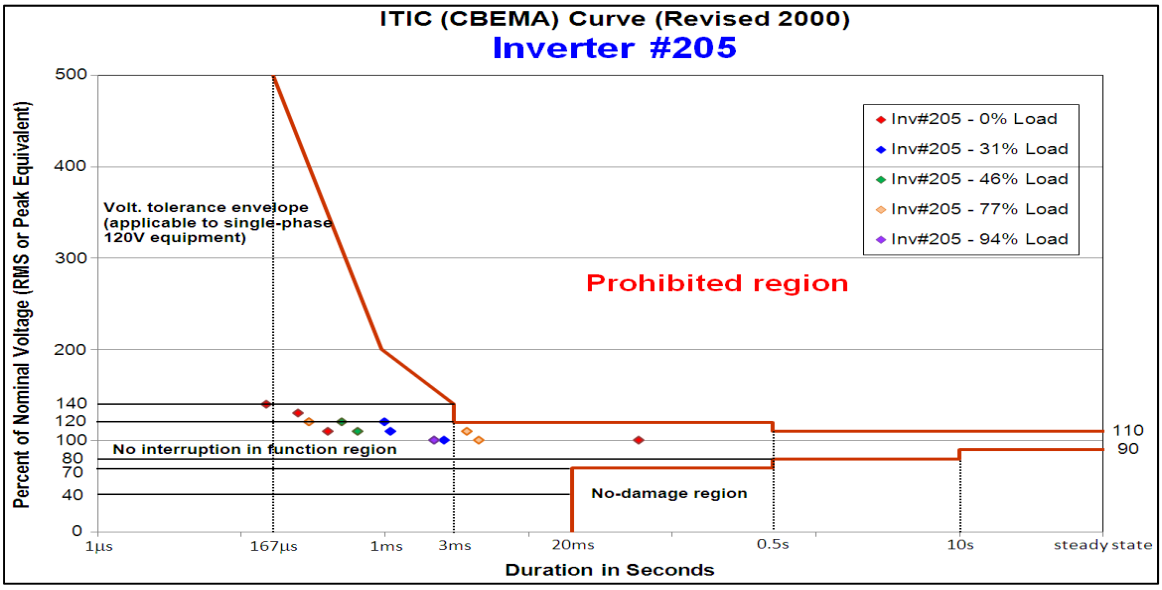

Figure 2.4.1 Inverter#205 TOV on ITIC (CBEMA)

The island of each test begins at the point where the voltage deviates from the normal steady state sinusoidal voltage waveform.

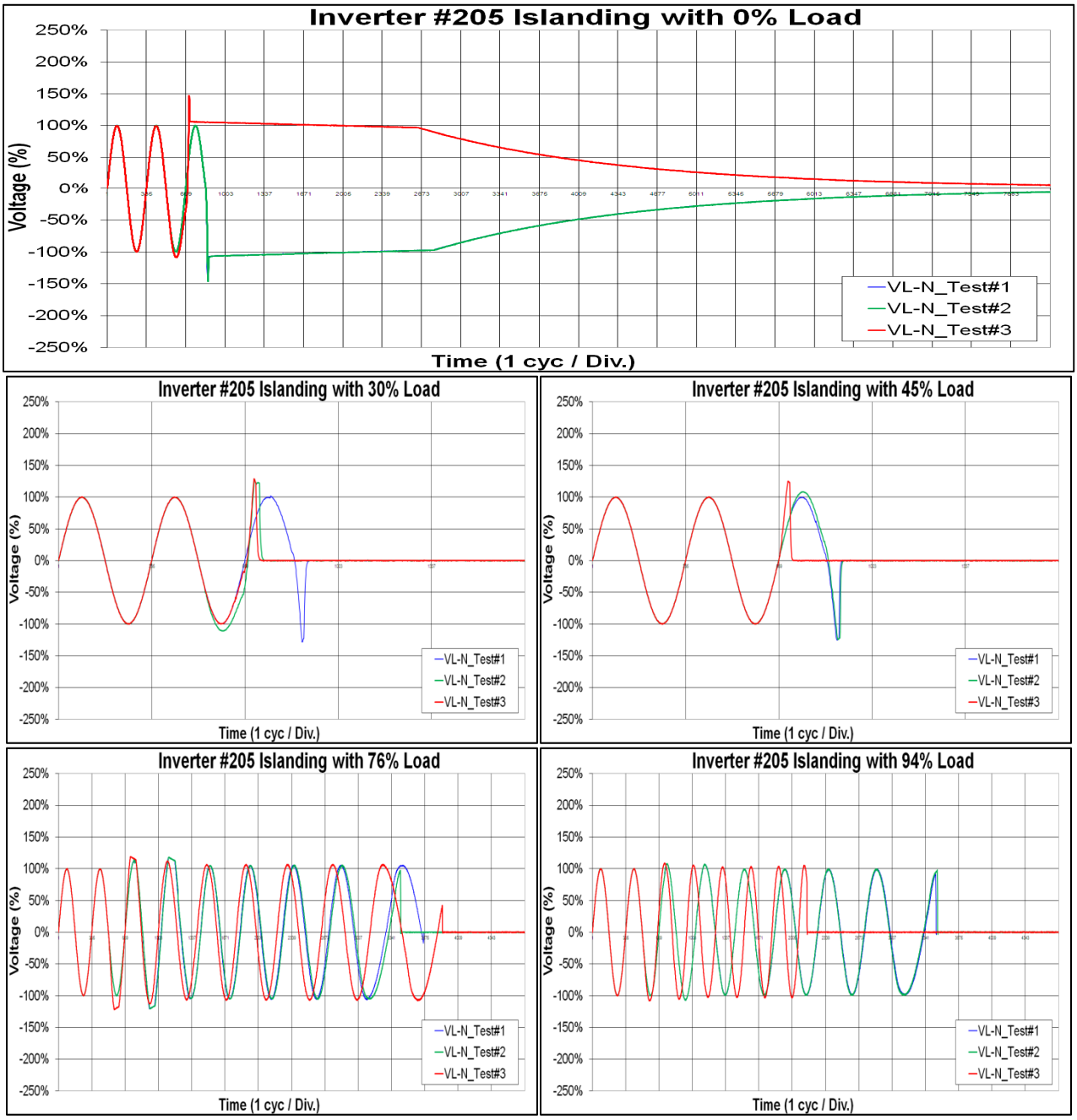

Figure 2.4.2 TOV During Grid Disconnection with Different Loads (Inverter #205)

2.5 Paralleled All Inverters

The Figure 2.5.1 and Figure 2.5.2 below show the behavior of Inverters 201, 202, 203, and 205 when operated in parallel and disconnected under the worst condition, with no load. Each test was performed several times as shown in the plots.

The key findings for this inverter are:

- Highest temporary overvoltage is 148% of nominal voltage and occurs when islanding with no load
- The maximum time when the voltage goes above 100% is less than 0.6 cycles
- Trips off within 11.5 cycles (within IEEE 1547 standard anti-islanding protection of 2 seconds)
- Negligible voltage discharge behavior when disconnected with no load
- The TOV generated from the paralleled inverters falls within the CBEMA curve when disconnected without load

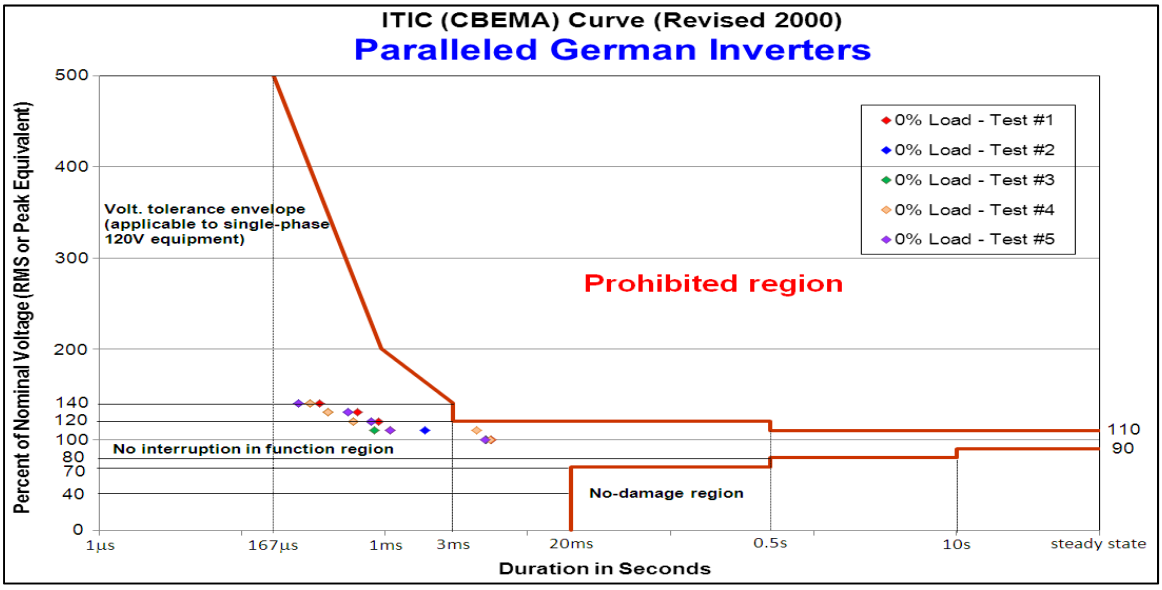

Figure 2.5.1 Paralleled Inverters TOV on ITIC (CBEMA)

The island of each test begins at the point where the voltage deviates from the normal steady state sinusoidal voltage waveform.

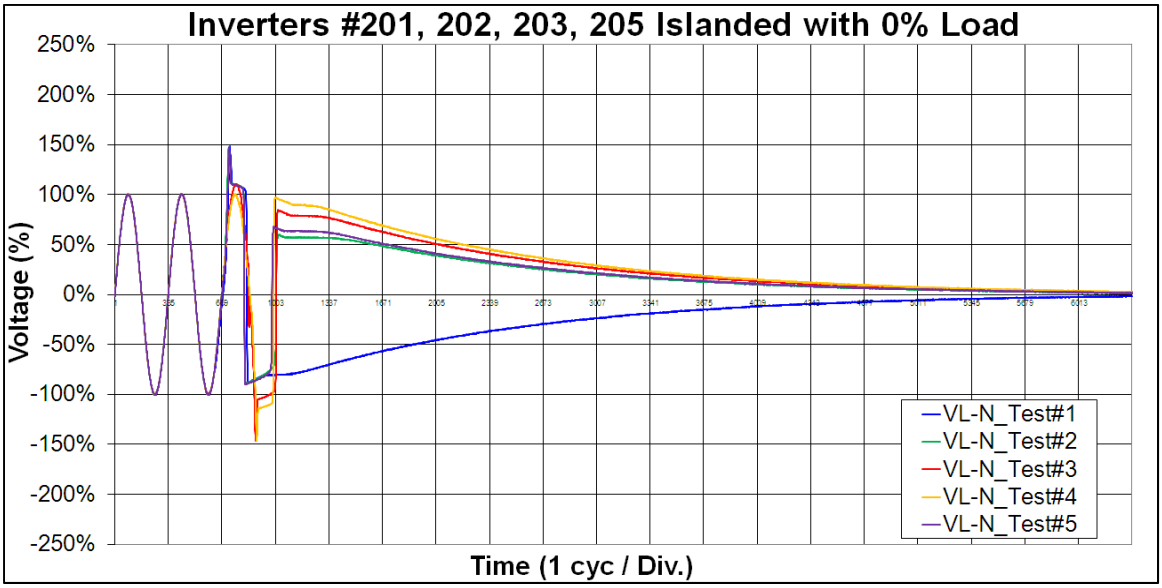

Figure 2.5.2 TOV During Grid Disconnection with Different Loads (Paralleled Inverters #201, 202, 203, 205)

3.0 FAULT CURRENT CONTRIBUTION

In order to assess their fault current contribution during system faults, the German inverters were physically shorted the hot line to ground when performing the following tests. Table 3.0.1 shows the detail behavior of this inverter during line to ground faults. The inverters were not tested for high impedance faults, which the voltage transient tests can provide additional information of the inverters behavior.

Key findings:

- Maximum fault current contribution ranges from 217% to 344% of nominal current within the first cycle of the inverters being shorted
- Maximum time to stop producing current (shutdown) ranges from 1.7 to 2.3 cycles
- Instantaneous fault current contributions (spikes) vary for an inverter tested multiple times
- Fault current behavior and dynamic performance is similar for all inverters tested

Manuf. #	Fault Type	Inverter #	PF	$I_{MAXIMUM-INSTANTANEOUS}$ (%)	$t_{MAXIMUM}$ (cycles) for I > 100%	$t_{MAXIMUM}$ (cycles) to trip off
4	Line-Gnd	201	Lead	333%	1.2	2.3
			Lag	344%	1.2	2.1
		202	Lead	327%	1.4	1.9
			Lag	298%	1.3	2.1
		203	Lead	311%	0.9	1.9
			Lag	289%	1.1	2.1
		205	Lead	245%	1.2	1.8
			Lag	217%	1.4	1.7

Table 3.0.1 Fault Current Contribution During Short Circuit

3.1. Inverter #201

Figure 3.1.1 indicates the behavior for Inverter 201 during various short circuit tests where its output was physically shorted to ground.

- Maximum instantaneous fault current is 344% of nominal current for less than 1 cycle
- The longest short circuit current time above 100% of rated current is 1.2 cycles
- The longest short circuit current time to shutdown is 2.3 cycles

The inverter short circuit begins where the sinusoidal current deviates from the normal sinusoidal current waveform.

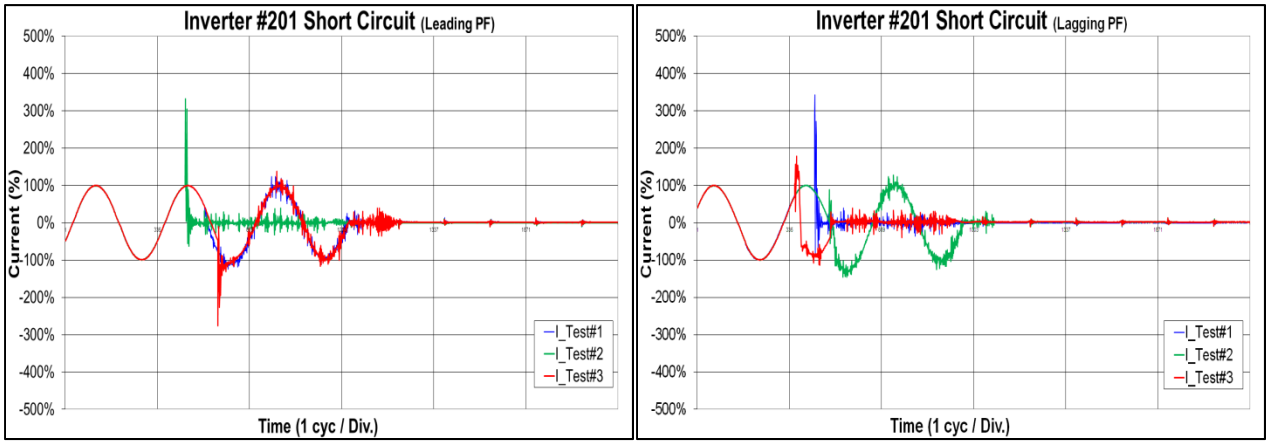

Figure 3.1.1 Fault Current Contribution (Inverter #201)

3.2. Inverter #202

Figure 3.2.1 below indicates the behavior for Inverter 202 during various short circuit tests where its output was physically shorted to ground.

- Maximum instantaneous fault current is 327% of nominal current for less than 1 cycle
- The longest short circuit current time above 100% of rated current is 1.4 cycles
- The longest short circuit current time to shutdown is 2.1 cycles

The inverter short circuit begins where the sinusoidal current deviates from the normal sinusoidal current waveform.

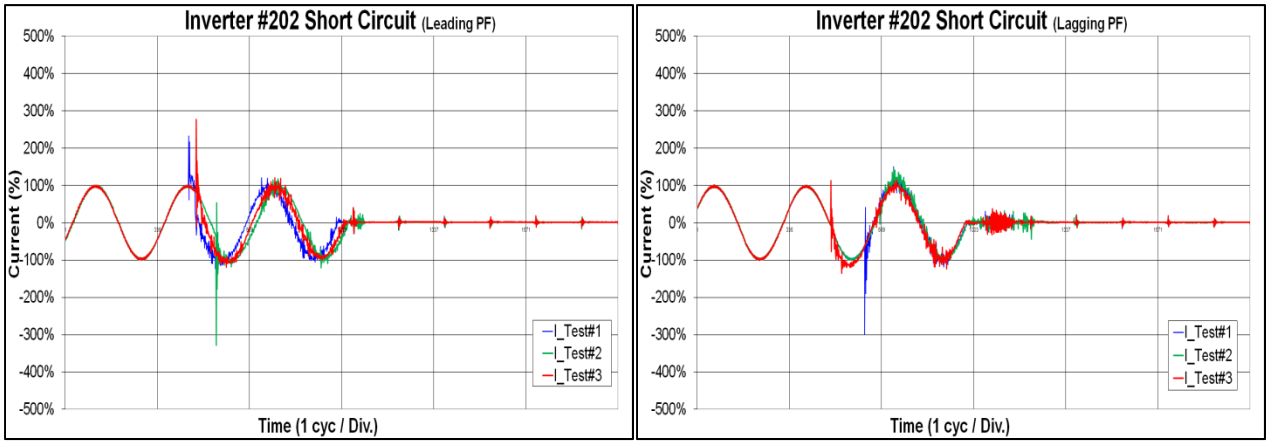

Figure 3.2.1 Fault Current Contribution (Inverter #202)

3.3. Inverter #203

Figure 3.3.1 below indicates the behavior for Inverter 203 during various short circuit tests where its output was physically shorted to ground.

- Maximum instantaneous fault current is 311% of nominal current for less than 1 cycle
- The longest short circuit current time above 100% of rated current is 1.1 cycles
- The longest short circuit current time to shutdown is 2.1 cycles

The inverter short circuit begins where the sinusoidal current deviates from the normal sinusoidal current waveform.

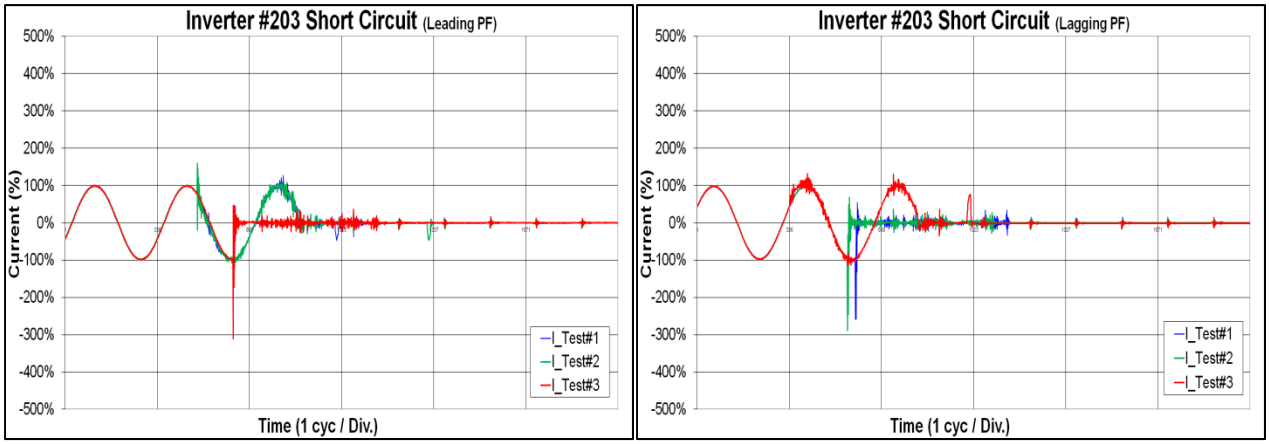

Figure 3.3.1 Fault Current Contribution (Inverter #203)

3.4. Inverter #205

Figure 3.4.1 below indicates the behavior for Inverter 205 during various short circuit tests where its output was physically shorted to ground.

- Maximum instantaneous fault current is 245% of nominal current for less than 1 cycle
- The longest short circuit current time above 100% of rated current is 1.4 cycles
- The longest short circuit current time to shutdown is 1.8 cycles

The inverter short circuit begins where the sinusoidal current deviates from the normal sinusoidal current waveform.

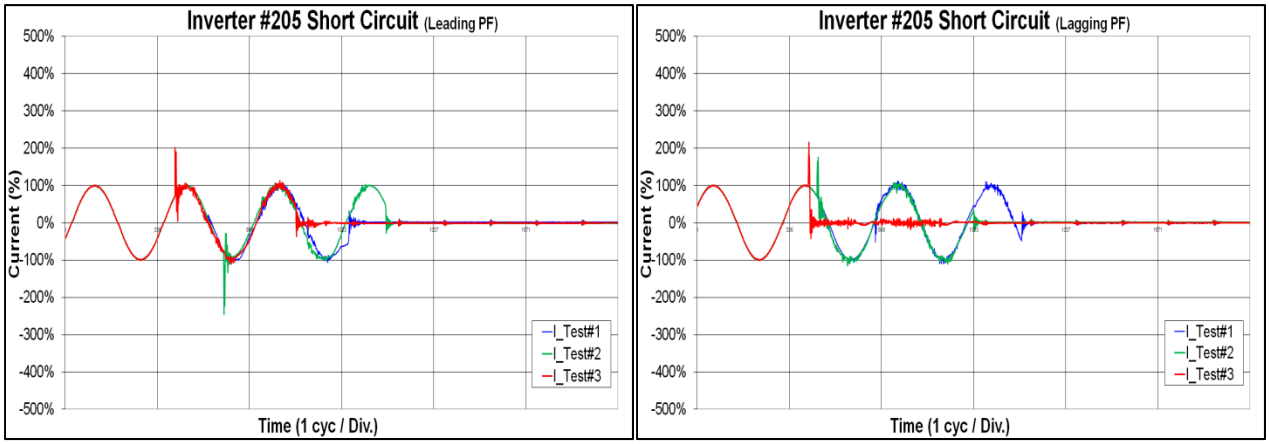

Figure 3.4.1 Fault Current Contribution (Inverter #205)

3.5. Paralleled All Inverters

Figure 3.5.1 below indicates the behavior for Inverter 205 during various short circuit tests where its output was physically shorted to ground.

- Maximum instantaneous fault current is 141% of nominal current for less than 1 cycle
- The longest short circuit current time above 100% of rated current is 0.6 cycles
- The longest short circuit current time to shutdown is 1.9 cycles

The inverter short circuit begins where the sinusoidal current deviates from the normal sinusoidal current waveform.

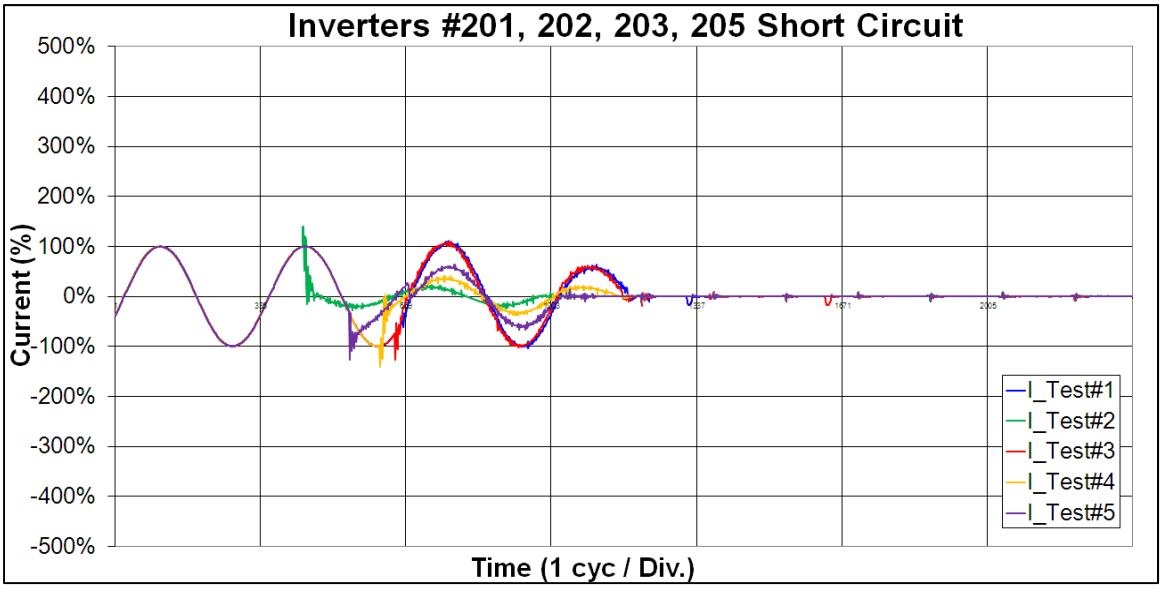

Figure 3.5.1 Fault Current Contribution (Paralleled Inverters #201, 202, 203, 205)

4.0 HARMONICS GENERATION

High sampling sinusoidal waveform data (1 million samples per second) was captured at the output of the inverters during normal operation, with resistive load, to assess their harmonics contribution. Table 4.0.1 below summarizes the harmonics contribution for all the tested inverters including inverters that follow U.S. standards. In addition, Figure 4.0.1 and Figure 4.0.2 display the individual harmonics as well as the total harmonic distortion (THD) for these inverters.

- All German inverters harmonics below the 35th harmonic are within the IEEE 1547 recommendations
- THD of all the German inverters is well below the IEEE 1547 recommendations (less than half)
- Inverter 202 and 203 showed a significant increase in voltage THD when calculated up to the 700th harmonic as opposed to calculated up to the 100th harmonic (more than 3 times larger)
- Inverter 202 showed a significant increase in current THD when calculated up to the 700th harmonic as opposed to calculated up to the 100th harmonic

Inverter #	Manuf.	Voltage Harmonics (% of Fundamental)						Current Harmonics (% of Fundamental)						THD (up to 100th)		THD (up to 700th)	
		3rd	5th	7th	9th	11th	13th	3rd	5th	7th	9th	11th	13th	V	I	V	I
1	1	0.05	0.17	0.11	0.03	0.07	0.04	0.37	0.23	0.06	0.10	0.16	0.16	0.36	0.80	1.07	2.36
2		0.11	0.17	0.06	0.03	0.06	0.10	0.29	0.14	0.16	0.17	0.19	0.20	0.44	0.92	0.95	1.91
3	2	0.33	0.19	0.02	0.02	0.06	0.06	2.93	0.53	0.19	0.08	0.04	0.02	0.44	3.97	0.48	3.98
8		0.13	0.12	0.12	0.10	0.06	0.06	1.55	0.60	0.35	0.33	0.35	0.32	0.41	2.91	0.51	3.02
11		0.11	0.10	0.11	0.11	0.09	0.05	2.35	0.47	0.37	0.27	0.16	0.06	0.32	3.34	0.36	3.37
4	3	0.04	0.13	0.08	0.08	0.12	0.09	1.03	0.74	0.67	0.50	0.34	0.27	0.33	1.89	0.45	2.01
5		0.17	0.12	0.19	0.12	0.10	0.10	1.24	0.94	0.71	0.54	0.42	0.31	0.43	2.15	0.50	2.19
6	4	0.17	0.12	0.09	0.08	0.09	0.07	1.24	0.66	0.43	0.31	0.31	0.25	0.36	1.70	0.39	1.75
7		0.18	0.11	0.10	0.15	0.17	0.16	1.16	0.48	0.43	0.51	0.48	0.42	0.55	1.79	0.62	1.86
12		0.02	0.15	0.09	0.03	0.08	0.06	0.72	0.32	0.26	0.29	0.20	0.14	0.37	1.22	0.43	1.33
10	6	0.29	0.11	0.05	0.02	0.09	0.06	1.50	0.25	1.43	1.09	0.59	0.56	0.39	4.13	0.61	5.12
13		0.13	0.10	0.14	0.02	0.06	0.12	1.35	0.30	0.39	0.39	0.21	0.34	0.38	2.05	0.58	2.67
14		0.07	0.13	0.06	0.11	0.06	0.04	1.43	0.32	0.27	0.38	0.17	0.19	0.34	2.04	0.56	2.41
16	7	0.04	0.25	0.28	0.27	0.24	0.22	1.03	1.65	1.22	1.06	0.82	0.65	0.64	2.90	0.83	3.05
101	8	0.03	0.02	0.04	0.04	0.04	0.04	1.29	0.60	0.30	0.53	0.44	0.35	0.12	1.79	0.25	1.99
102		0.03	0.01	0.04	0.04	0.04	0.03	1.26	0.34	0.08	0.31	0.20	0.24	0.11	1.48	0.24	1.60
103	9	0.03	0.02	0.04	0.04	0.05	0.04	3.82	0.78	0.64	0.52	0.36	0.25	0.13	4.03	0.27	4.38
104		0.02	0.02	0.04	0.04	0.04	0.03	0.32	0.16	0.15	0.10	0.11	0.10	0.11	0.50	0.25	0.83
105	4	0.05	0.06	0.02	0.05	0.02	0.03	0.80	0.23	0.32	0.31	0.37	0.34	0.29	1.92	0.39	1.95
201	4	0.04	0.04	0.03	0.02	0.02	0.01	1.51	0.33	0.25	0.23	0.18	0.15	0.09	2.00	0.15	2.02
202		0.03	0.03	0.03	0.03	0.04	0.03	0.71	0.24	0.16	0.15	0.16	0.16	0.11	1.41	0.44	2.47
203		0.03	0.04	0.03	0.02	0.02	0.02	0.72	0.19	0.12	0.08	0.11	0.10	0.10	1.35	0.35	1.57
205		0.03	0.01	0.02	0.03	0.03	0.04	0.94	0.23	0.22	0.20	0.16	0.15	0.10	1.08	0.19	1.28
IEEE 1547								4.00	4.00	4.00	4.00	2.00	2.00		5.00		5.00

Table 4.0.1 Harmonic Contribution from Residential Inverters

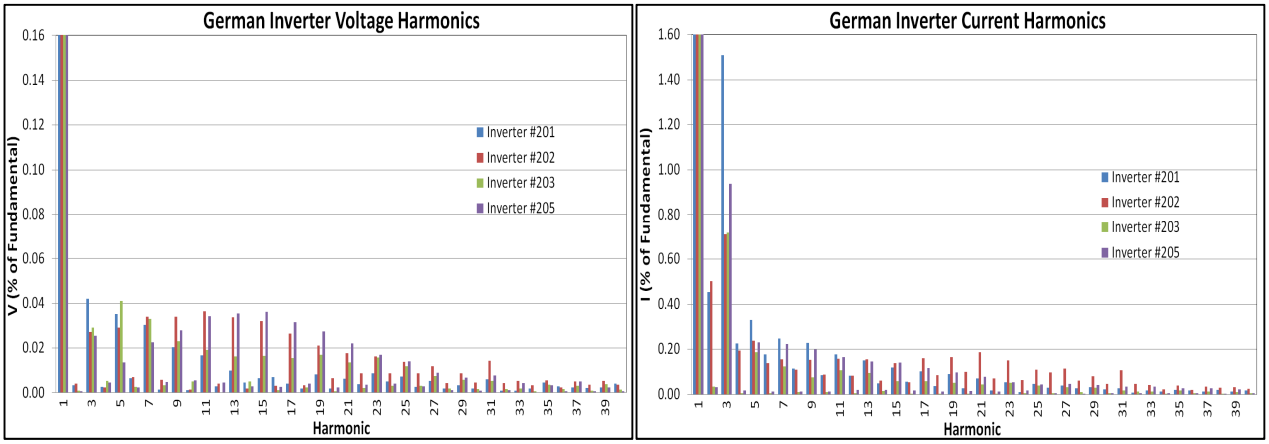

Figure 4.0.1 Voltage & Current Harmonics (1st - 40th)

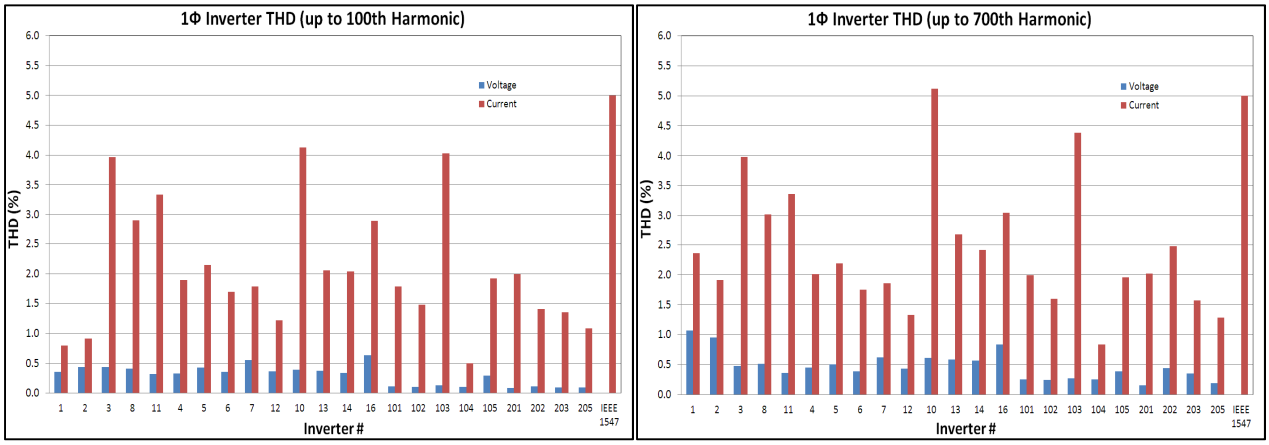

Figure 4.0.2 Voltage & Current Total Harmonic Distortion

4.1 Grid Simulator

The grid simulator harmonics contributions are shown in Figure 4.1.1 as a percentage of the fundamental. The grid simulator was operating with a light load.

- Individual voltage harmonics are less than 0.05% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.0199%)
  - H_{420} is the highest of the high order harmonics (0.0486%)
- Individual current harmonics are less than 0.6% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.53%)
  - H_{414} is the highest of the high order harmonics (0.15%)

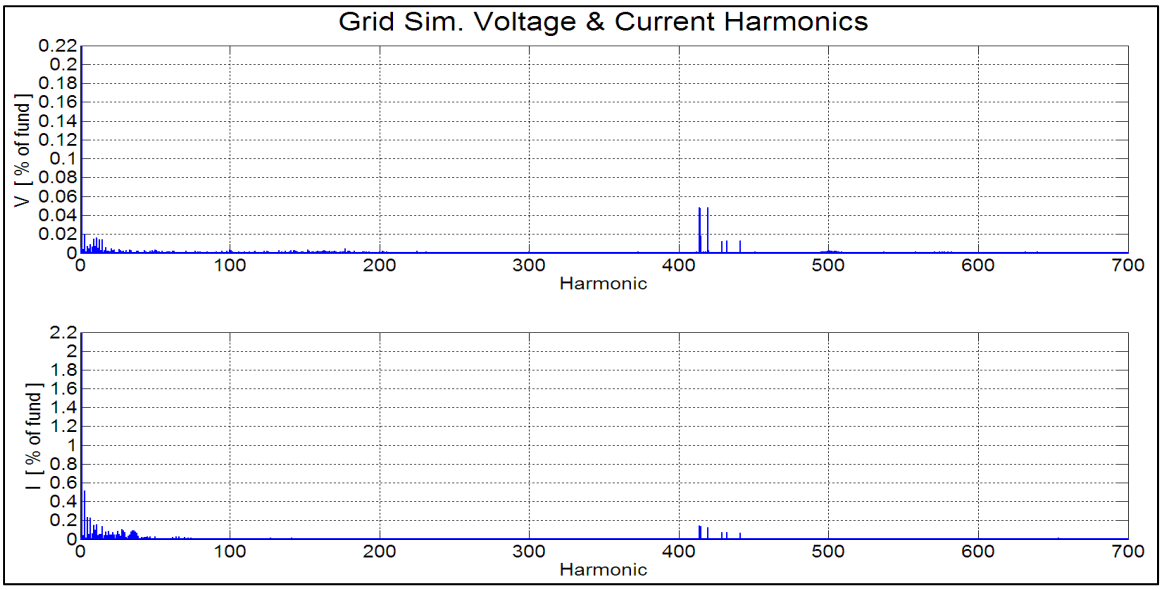

Figure 4.1.1 Harmonics Contribution (Grid Simulator)

4.2 Inverter #201

Figure 4.2.1 below represents the harmonics contribution of Inverter 201 measured as a percentage of the fundamental. The inverter was operating at full power output.

- Individual voltage harmonics are less than 0.05% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.0419%)
  - H_{268} is the highest of the high order harmonics (0.0425%)
- Individual current harmonics are less than 1.6% of the fundamental
  - H_3 is the highest of the lower order harmonics (1.51%)
  - H_{266} is the highest of the high order harmonics (0.16%)

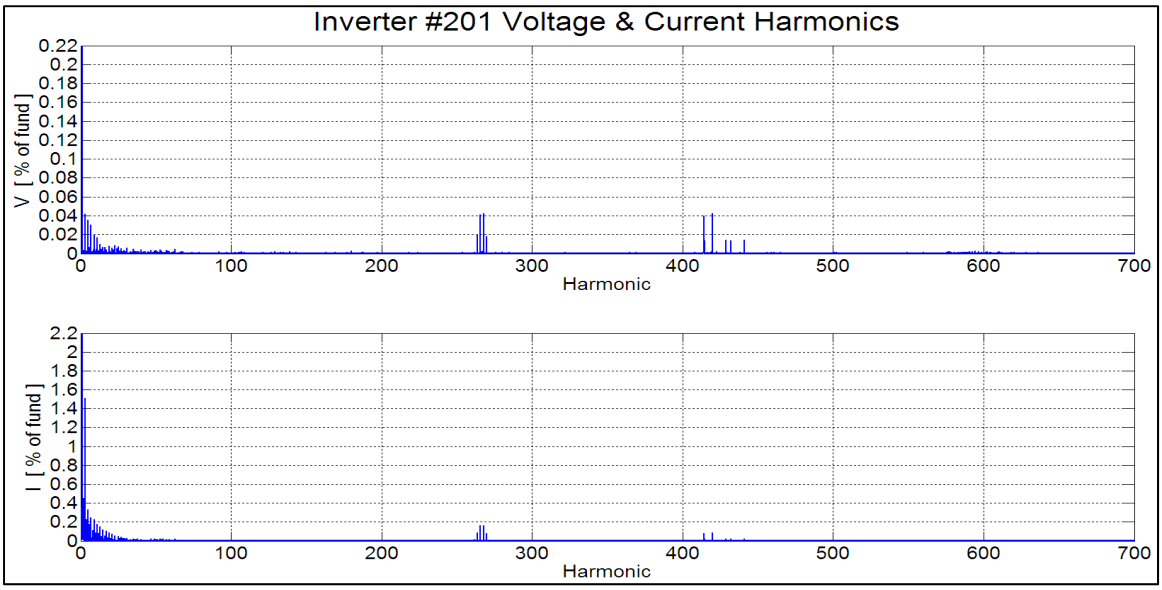

Figure 4.2.1 Harmonics Contribution (Inverter #201)

4.3 Inverter #202

The harmonics contributions from Inverter 202 are shown in Figure 4.3.1 as a percentage of the fundamental. The inverter was operating at full power output.

- Individual voltage harmonics are less than 0.2% of the fundamental
  - H_{11} is the highest of the lower order harmonics (0.0364%)
  - H_{268} is the highest of the high order harmonics (0.1939%)
- Individual current harmonics are less than 1% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.71%)
  - H_{266} is the highest of the high order harmonics (0.94%); that is above IEEE 1547 recommendations

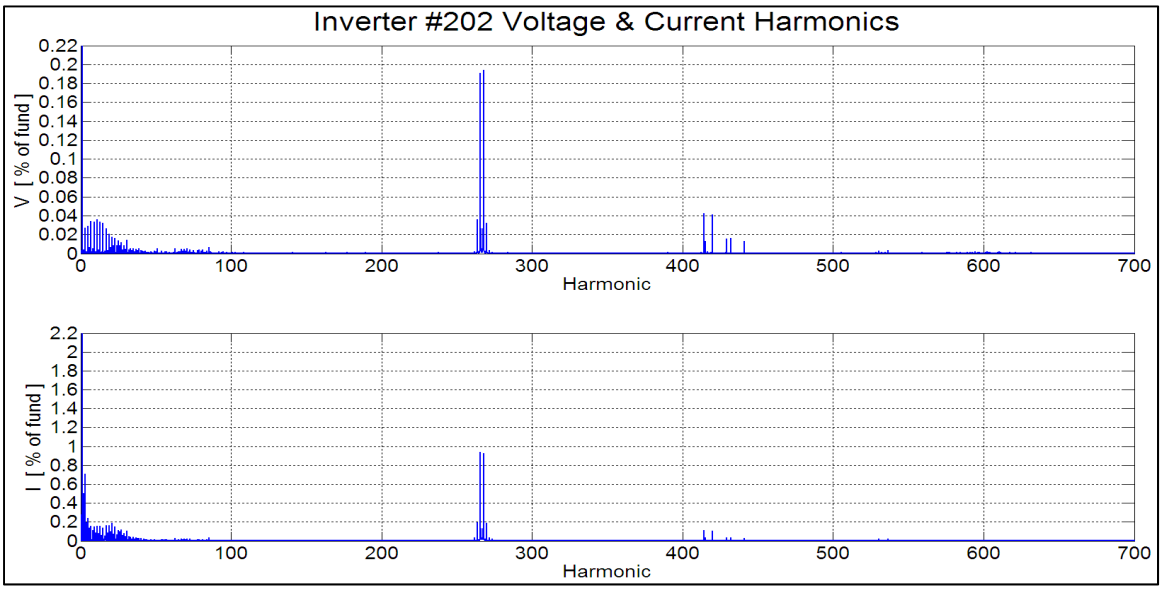

Figure 4.3.1 Harmonics Contribution (Inverter #202)

4.4 Inverter #203

Figure 4.4.1 below have the harmonics contribution of Inverters 203 measured as a percentage of the fundamental. The inverter was operating at full power output.

- Individual voltage harmonics are less than 0.22% of the fundamental
  - H_5 is the highest of the lower order harmonics (0.0411%)
  - H_{268} is the highest of the high order harmonics (0.2164%)
- Individual current harmonics are less than 0.8% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.72%)
  - H_{268} is the highest of the high order harmonics (0.53%); that is above IEEE 1547 recommendations

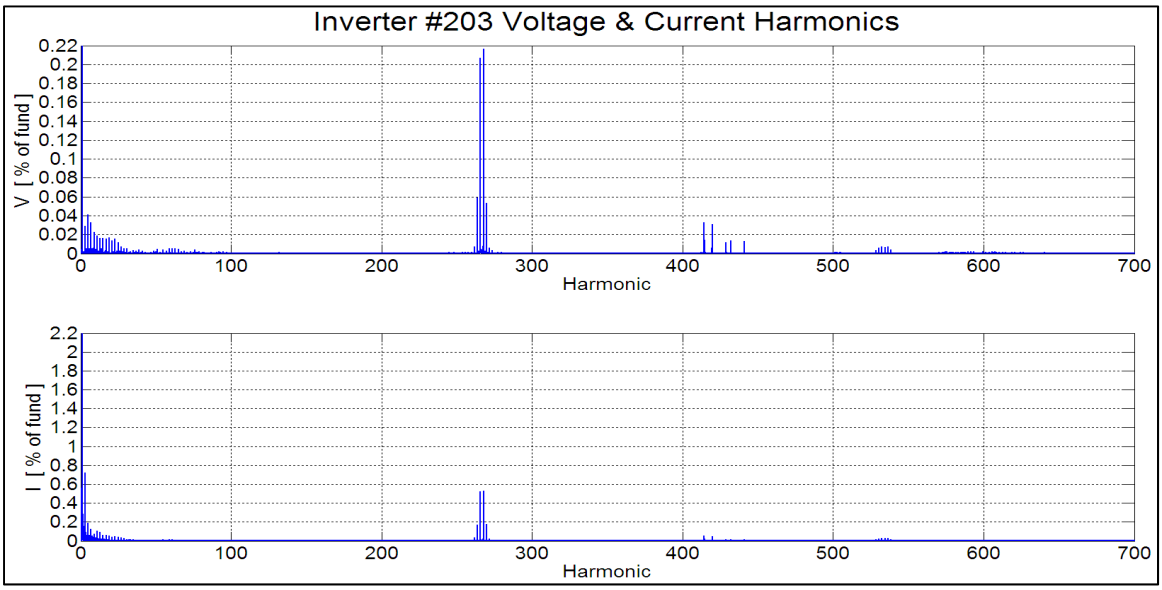

Figure 4.4.1 Harmonics Contribution (Inverter #203)

4.5 Inverter #205

The harmonics contribution from Inverters 205 is shown in Figure 4.5.1 as a percentage of the fundamental. The inverter was operating at full power output.

- Individual voltage harmonics are less than 0.06% of the fundamental
  - H_{15} is the highest of the lower order harmonics (0.0362%)
  - H_{268} is the highest of the high order harmonics (0.0554%)
- Individual current harmonics are less than 1% of the fundamental
  - H_3 is the highest of the lower order harmonics (0.94%)
  - H_{268} is the highest of the high order harmonics (0.32%); that is above IEEE 1547 recommendations

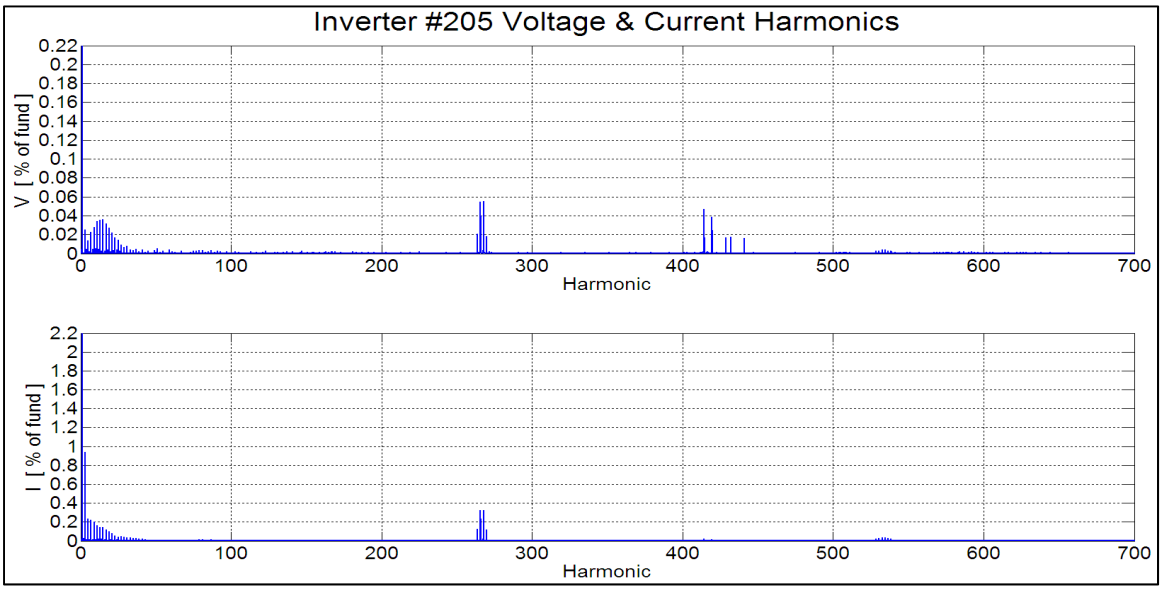

Figure 4.5.1 Harmonics Contribution (Inverter #205)

5.0 VOLTAGE RAMP

The grid voltages were ramped down and up while maintaining constant load in order to assess the inverters behavior at various voltage levels, specifically the response of the current and active power. Table 5.0.1 and 0 below summarize the deviation in current and active power caused by the voltage ramping.

- All German inverters attempt to maintain constant active power (P) during lower or higher voltages
- Inverters 201 and 203 began exhibiting constant current behavior once they reached their respective maximum current output limits
- German inverters displayed a fast current response resulting in negligible power deviations

Manuf. #	Inverter #	$V_{DEVIATION}$ (± %)	t_{RAMP} (sec)	$I_{DEVIATION}$ (± %)	$P_{DEVIATION}$ (± %)	Comments
4	201	-10%	4	+3%	-7%	Constant power until current limit, then constant current
			8	+3%	-7%	Constant power until current limit, then constant current
	202		4	+10%	-1% , +0%	Constant power
			8	+10%	-1% , +0%	Constant power
	203		4	+2%	-8%	Constant power until current limit, then constant current
			8	+2%	-8%	Constant power until current limit, then constant current
	205		4	+11%	-0% , +0%	Constant Power
			8	+11%	-0% , +0%	Constant Power

Table 5.0.1 Voltage Ramp Down Response (-10% Voltage Deviation)

Manuf. #	Inverter #	$V_{DEVIATION}$ (± %)	t_{RAMP} (sec)	$I_{DEVIATION}$ (± %)	$P_{DEVIATION}$ (± %)	Comments
4	201	-10%	4	-9%	+1% , -0%	Constant Power
			8	-9%	+1% , -0%	Constant Power
	202		4	-9%	+1% , -0%	Constant Power
			8	-9%	+1% , -0%	Constant Power
	203		4	-9%	+1% , -2%	Constant Power
			8	-9%	+1% , -0%	Constant Power
	205		4	-9%	+0% , -0%	Constant Power
			8	-9%	+0% , -0%	Constant Power

Table 5.0.2 Voltage Ramp Up Response (+10% Voltage Deviation)

5.1 Inverter #201

Voltage Ramps Down 10%

Figure 5.1.1 below indicates the behavior for Inverter 201 during voltage ramp-down tests.

- Current ramps up until it reaches its maximum output limit, 3% above its nominal rating
- Current remains relatively constant at its output limit until voltage recovers within 3% of nominal
- Active power (P) ramps down 7% below nominal while current is constant

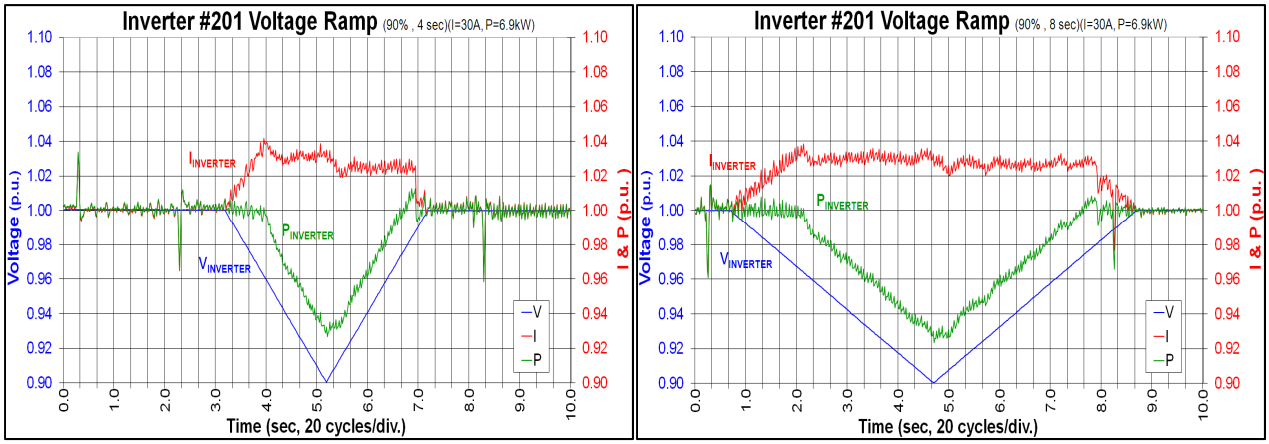

Figure 5.1.1 Voltage Ramp Down Response (Inverter #201)

Voltage Ramps Up 10%

Figure 5.1.2 below indicates the behavior for Inverter 201 during voltage ramp-up tests.

- Current ramps down to 9% below nominal and ramps up to maintain constant active power (P)
- Active power (P) deviation is minimal, within 1% of its nominal value

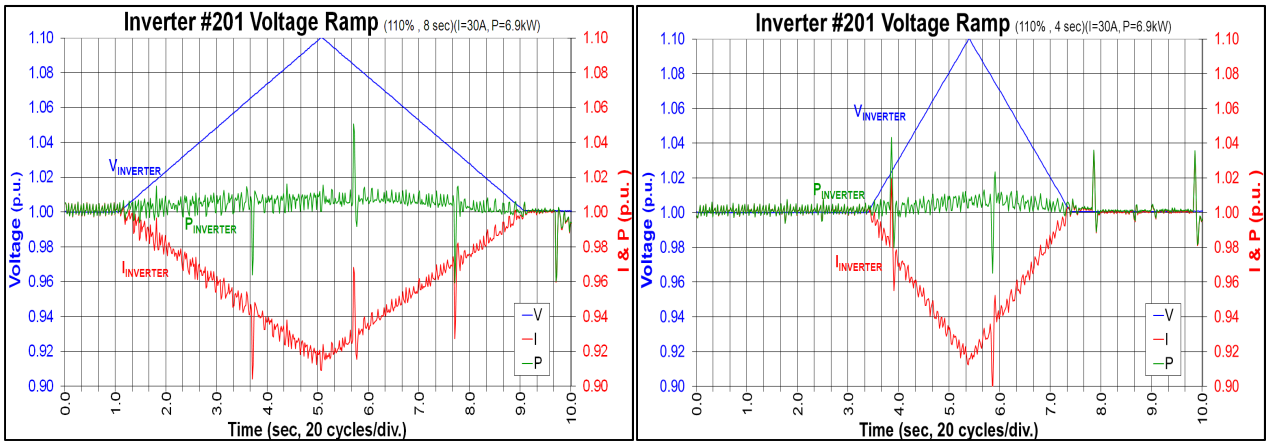

Figure 5.1.2 Voltage Ramp Up Response (Inverter #201)

5.2 Inverter #202

Voltage Ramps Down 10%

Inverter 202 behavior during voltage ramp-down tests is shown in Figure 5.2.1.

- Current ramps up to 10% above its nominal rating to maintain constant active power (P)
- Active power (P) remains constant within 1% of nominal output
- The maximum output current limit for inverter 202 is reached at 10% above nominal

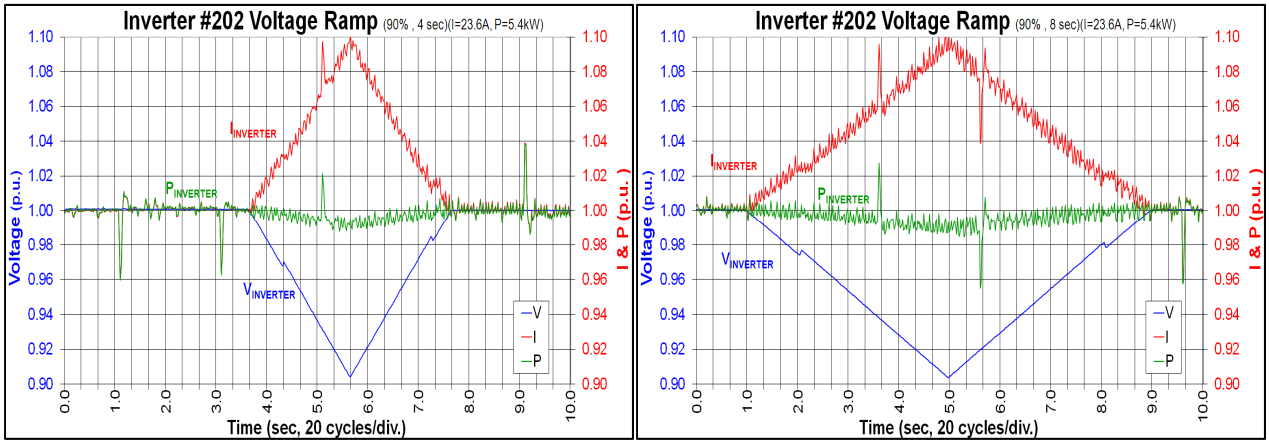

Figure 5.2.1 Voltage Ramp Down Response (Inverter #202)

Voltage Ramps Up 10%

Inverter 202 behavior during voltage ramp-up tests is shown in Figure 5.2.2.

- Current ramps down to 9% below nominal and ramps up to maintain constant active power (P)
- Active power (P) deviation is minimal, within 1% of its nominal value

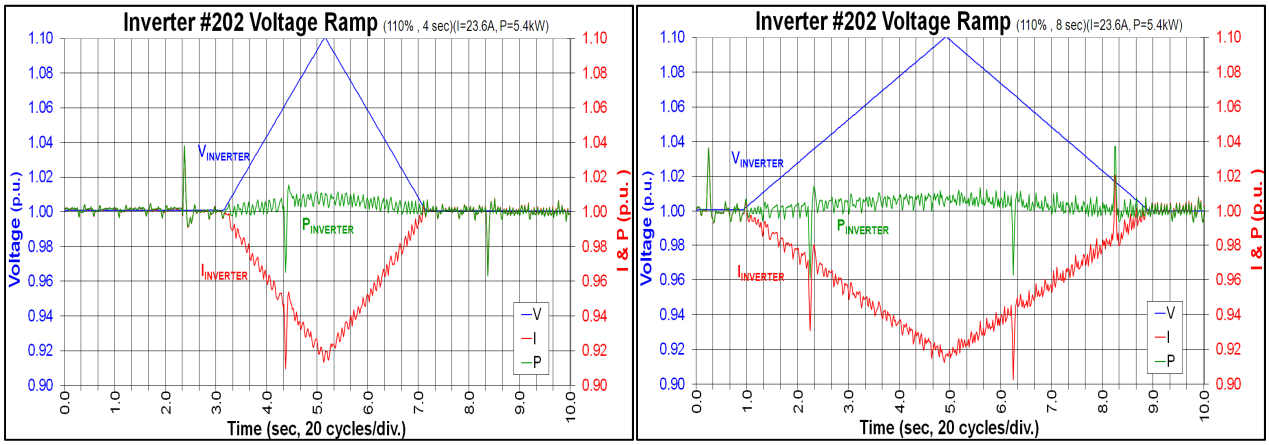

Figure 5.2.2 Voltage Ramp Up Response (Inverter #202)

5.3 Inverter #203

Figure 5.3.1 below indicates the behavior for Inverter 203 during voltage ramp-down tests.

Voltage Ramps Down 10%

- Current ramps up until it reaches its maximum output limit, 2% above its nominal rating
- Current remains relatively constant at its output limit until voltage recovers within 2% of nominal
- Active power (P) ramps down 8% below nominal while current is constant

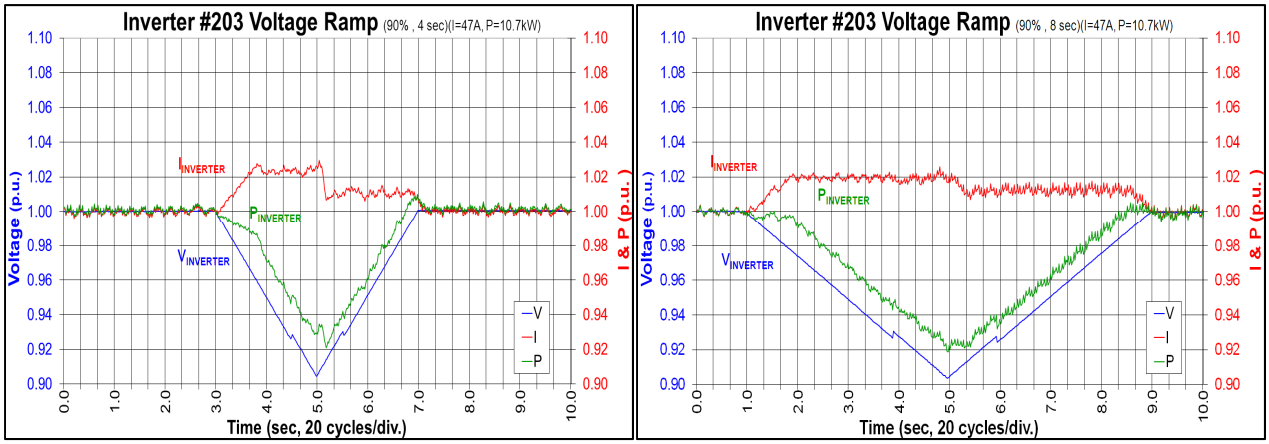

Figure 5.3.1 Voltage Ramp Down Response (Inverter #203)

Voltage Ramps Up 10%

Figure 5.3.2 below indicates the behavior for Inverter 203 during voltage ramp-up tests.

- Current ramps down to 9% below nominal and ramps up to maintain constant active power (P)
- Active power (P) deviation is minimal, within 2% of its nominal value

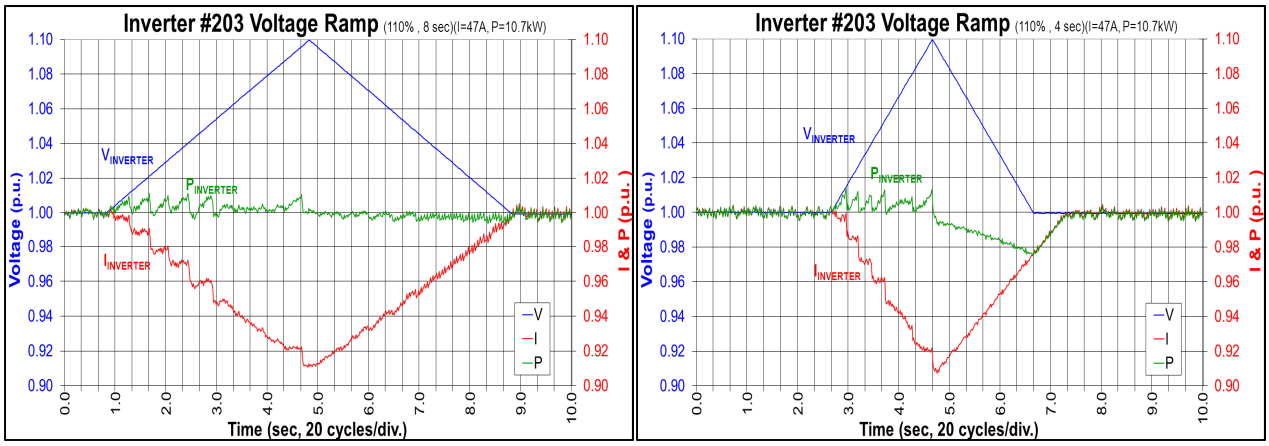

Figure 5.3.2 Voltage Ramp Up Response (Inverter #203)

5.4 Inverter #205

Voltage Ramps Down 10%

Inverter 205 behavior during voltage ramp-down tests is shown in Figure 5.4.1.

- Current ramps up to 11% above its nominal rating to maintain constant active power (P)
- ♦ Active power (P) remains constant within 1% of nominal output
- ♦ The maximum output current limit for inverter 205 is reached at 11% above nominal

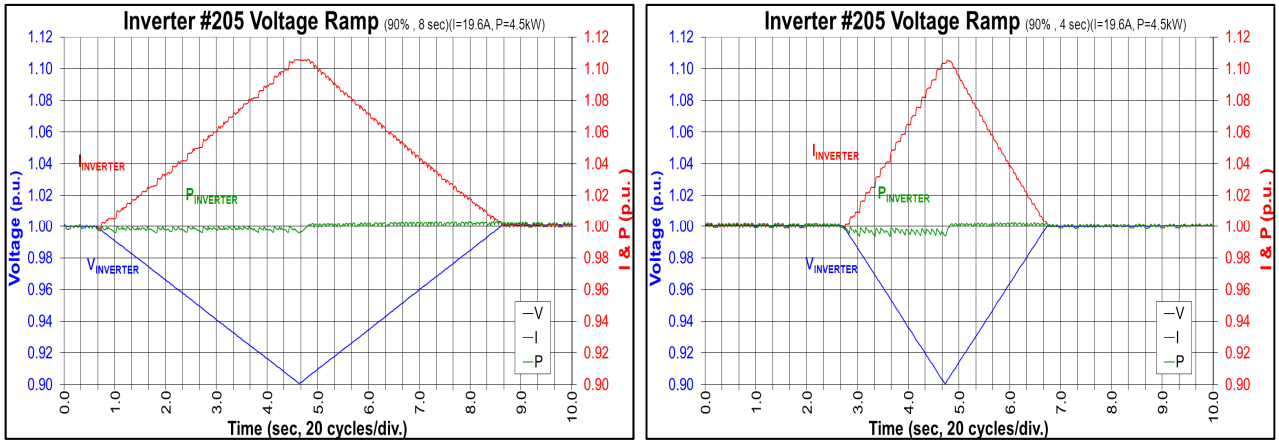

Figure 5.4.1 Voltage Ramp Down Response (Inverter #205)

Voltage Ramps Up 10%

Inverter 205 behavior during voltage ramp-up tests is shown in Figure 5.4.2.

- Current ramps down to 9% below nominal and ramps up to maintain constant active power (P)

♦ Active power (P) deviation is minimal due to an incredibly fast current response

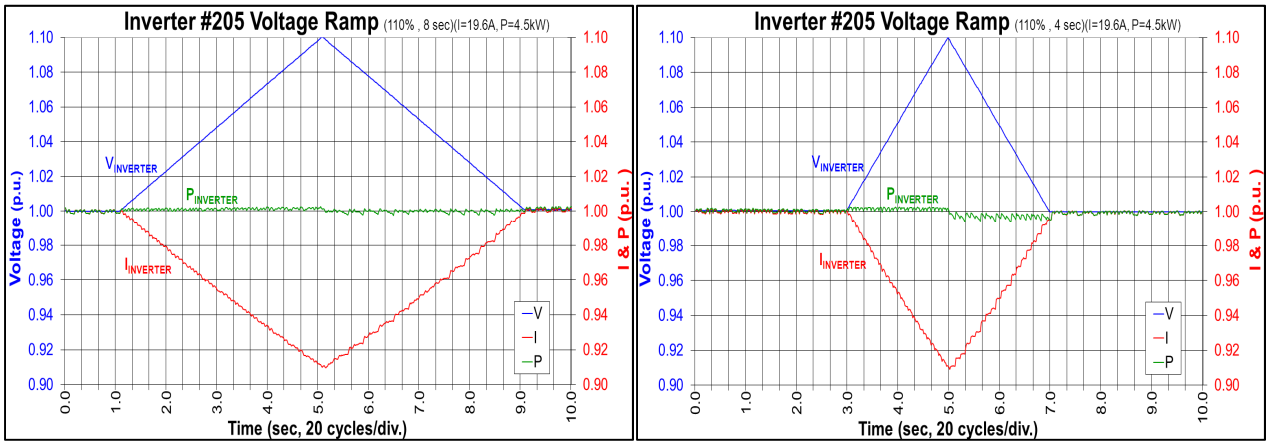

Figure 5.4.2 Voltage Ramp Up Response (Inverter #205)

6.0 FREQUENCY RAMP

The grid frequency was ramped down and up while maintaining constant load in order to assess the inverters behavior at various frequency levels, specifically the response of the current and active power. Table 6.0.1 below summarizes the deviation in current and active power caused by the frequency ramping.

- Frequency ramped down to 59 Hz and back to 60 Hz in 8 and 4 second intervals
- Under-frequency protection did not trip off any of the tested inverters
- All German inverters maintain nearly constant current and active power (P) at lower frequencies

Manuf. #	Inverter #	$V_{DEVIATION}$ (Hz)	t_{RAMP} (sec)	$I_{DEVIATION}$ (± %)	$P_{DEVIATION}$ (± %)	Comments
4	201	59.0	4	+2%	+1%	Negligible Current/Power Deviation
			8	+1%	+1%	Negligible Current/Power Deviation
	202		4	+2%	+1%	Negligible Current/Power Deviation
			8	+1%	+1%	Negligible Current/Power Deviation
	203		4	±1%	±1%	Negligible Current/Power Deviation
			8	±1%	±1%	Negligible Current/Power Deviation
	205		4	±0%	±1%	Negligible Current/Power Deviation
			8	±0%	±1%	Negligible Current/Power Deviation

Table 6.0.1 Frequency Ramp Response (-1 Hz Deviation)

6.1 Inverter #201

Figure 6.1.1 below indicates the behavior for Inverter 201 during frequency ramping tests.

- Negligible changes in current output (within 2% of nominal) and power output (within 1% of nominal)

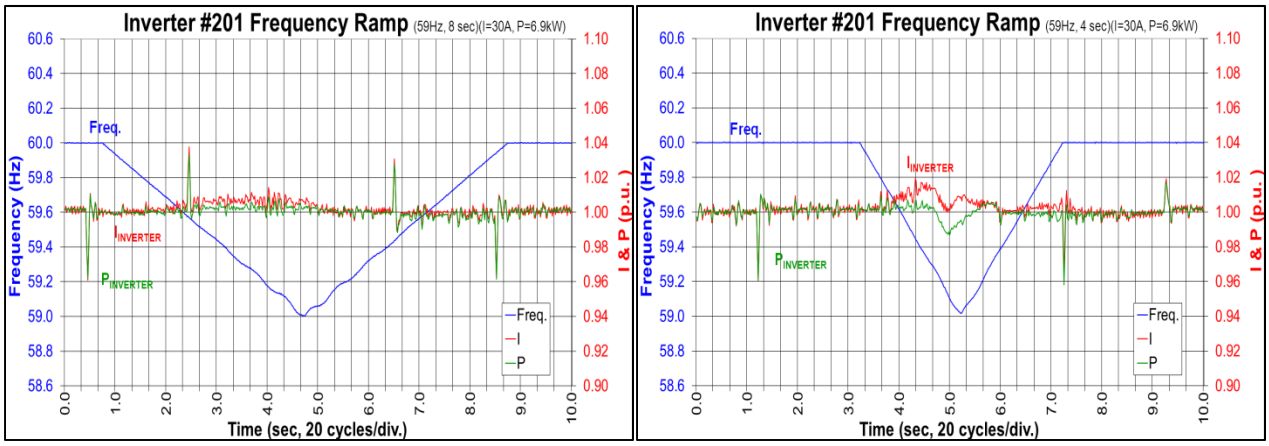

Figure 6.1.1 Frequency Ramp Response (Inverter #201)

6.2 Inverter #202

The Inverter 202 behavior during frequency ramping tests is shown in Figure 6.2.1.

- Negligible changes in current output (within 2% of nominal) and power output (within 1% of nominal)

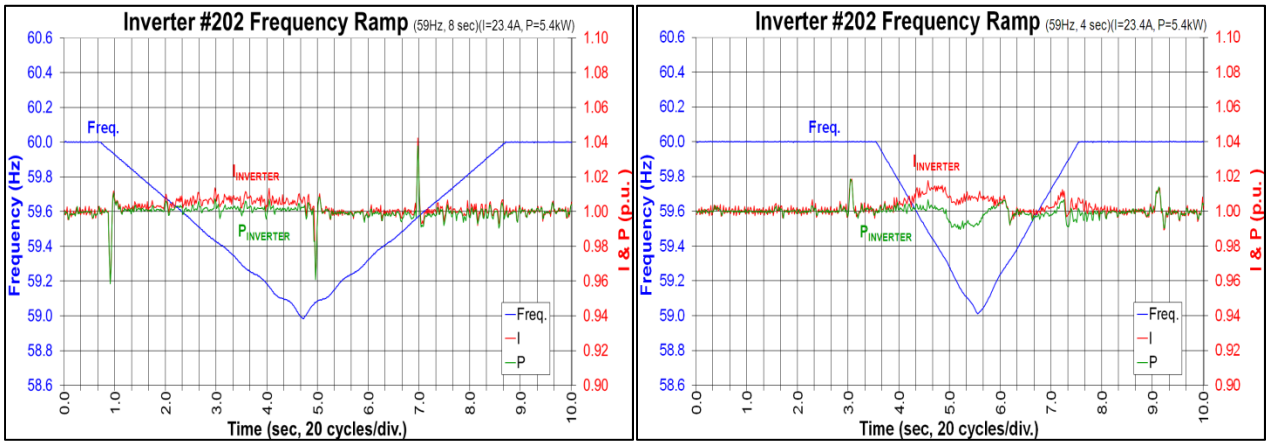

Figure 6.2.1 Frequency Ramp Response (Inverter #202)

6.3 Inverter #203

Figure 6.3.1 below indicates the behavior for Inverter 203 during frequency ramping tests.

- Negligible changes in current output (within 1% of nominal) and power output (within 1% of nominal)

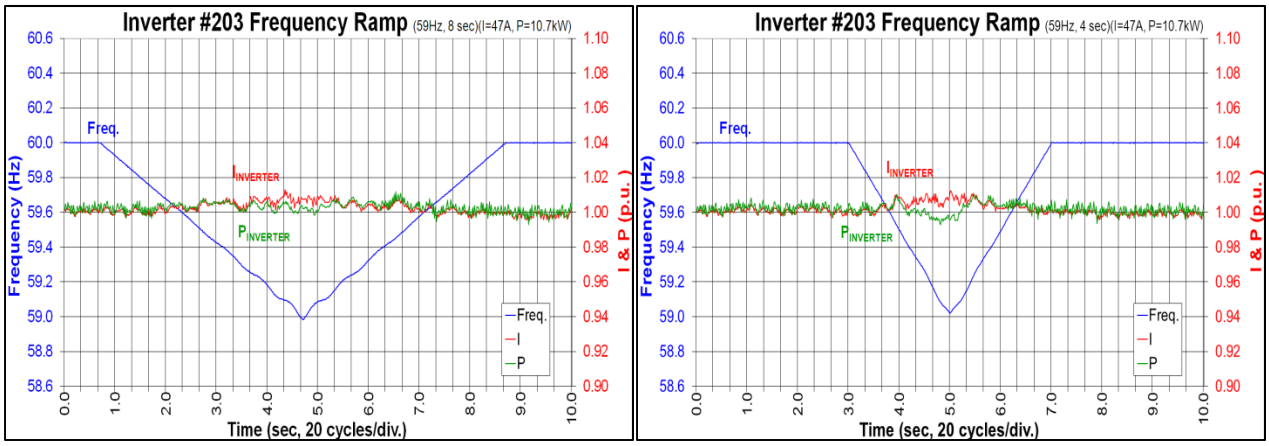

Figure 6.3.1 Frequency Ramp Response (Inverter #203)

6.4 Inverter #205

The Inverter 205 behavior during frequency ramping tests is shown in Figure 6.4.1.

- Negligible changes in current output (within 0.5% of nominal) and power output (within 1% of nominal)

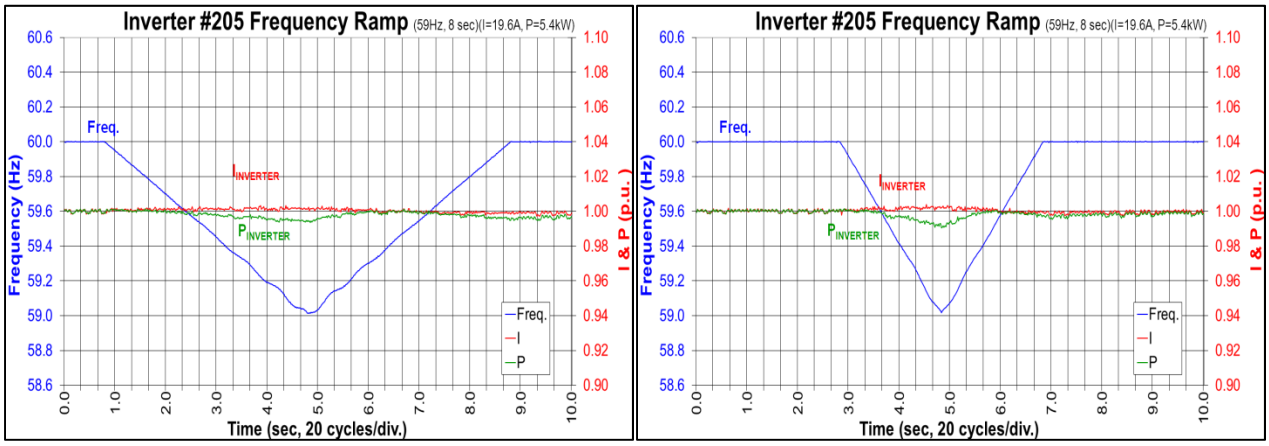

Figure 6.4.1 Frequency Ramp Response (Inverter #205)

7.0 VOLTAGE OSCILLATION

The grid voltage was oscillated between 100% and 90% to create voltage oscillations with swing frequencies of 0.25 Hz, 1 Hz, and 2 Hz. Table 7.0.1 summarizes the performance of all the tested inverters during voltage oscillations.

- All inverters attempt to dampen power oscillations by oscillating current opposite of the voltage
- Inverters 201 and 203 have a more difficult time maintaining constant power due to their respective maximum current output limits
- Current and power deviations typically increase at higher swing frequencies such as 1 Hz and 2 Hz

Manuf. #	Inverter #	f_{swing}	$I_{DEVIATION}$ (± %)	$P_{DEVIATION}$ (± %)	Comments
4	201	0.25 Hz	3% ~ 0%	0% ~ -7%	Current oscillates opposite to the voltage (limited to 103% current) / Power oscillates with voltage
		1.0 Hz	5% ~ -2%	1% ~ -8%	Current attempts to oscillate opposite to the voltage (delayed response) / Power oscillates with voltage
		2.0 Hz	3% ~ -3%	1% ~ -12%	Current attempts to oscillate opposite to the voltage (delayed response) / Power oscillates with voltage
	202	0.25 Hz	10% ~ 0%	0% ~ -1%	Current oscillates opposite to the voltage / minimal Power oscillations
		1.0 Hz	9% ~ 0%	3% ~ -4%	Current oscillates opposite to the voltage / minimal Power oscillations
		2.0 Hz	10% ~ -2%	2% ~ -3%	Current oscillates opposite to the voltage / minimal Power oscillations
	203	0.25 Hz	2% ~ 0%	0% ~ -8%	Current oscillates opposite to the voltage (limited to 102% current) / Power oscillates with volt.
		1.0 Hz	2% ~ -2%	0% ~ -9%	Current oscillates opposite to the voltage / Power oscillations with voltage
		2.0 Hz	2% ~ -4%	0% ~ -11%	Current oscillates opposite to the voltage / Power oscillations with voltage
	205	0.25 Hz	12% ~ 0%	2% ~ -1%	Current oscillates opposite to the voltage / minimal Power oscillations
		1.0 Hz	10% ~ 0%	2% ~ -3%	Current oscillates opposite to the voltage / Power oscillations result from distorted current profile
		2.0 Hz	12% ~ -7%	4% ~ -8%	Current oscillates opposite to the voltage / Power oscillations result from distorted current profile

Table 7.0.1 Voltage Oscillation Response (f_{swing} = 0.25, 1.0, 2.0 Hz)

7.1 Inverter #201

Figure 7.1.1 below indicates the behavior for Inverter 201 during voltage oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, and 2 Hz).

- Current responds fastest during 0.25 Hz oscillations to minimize power oscillations (P deviates by 7%)
- Continuous current output limit also clips the current to approximately 3% above nominal
- Larger power deviations (8%) occur during 1 Hz oscillations due to a slower current response
- Largest power deviations (12%) occur during 2 Hz oscillations from delayed current response

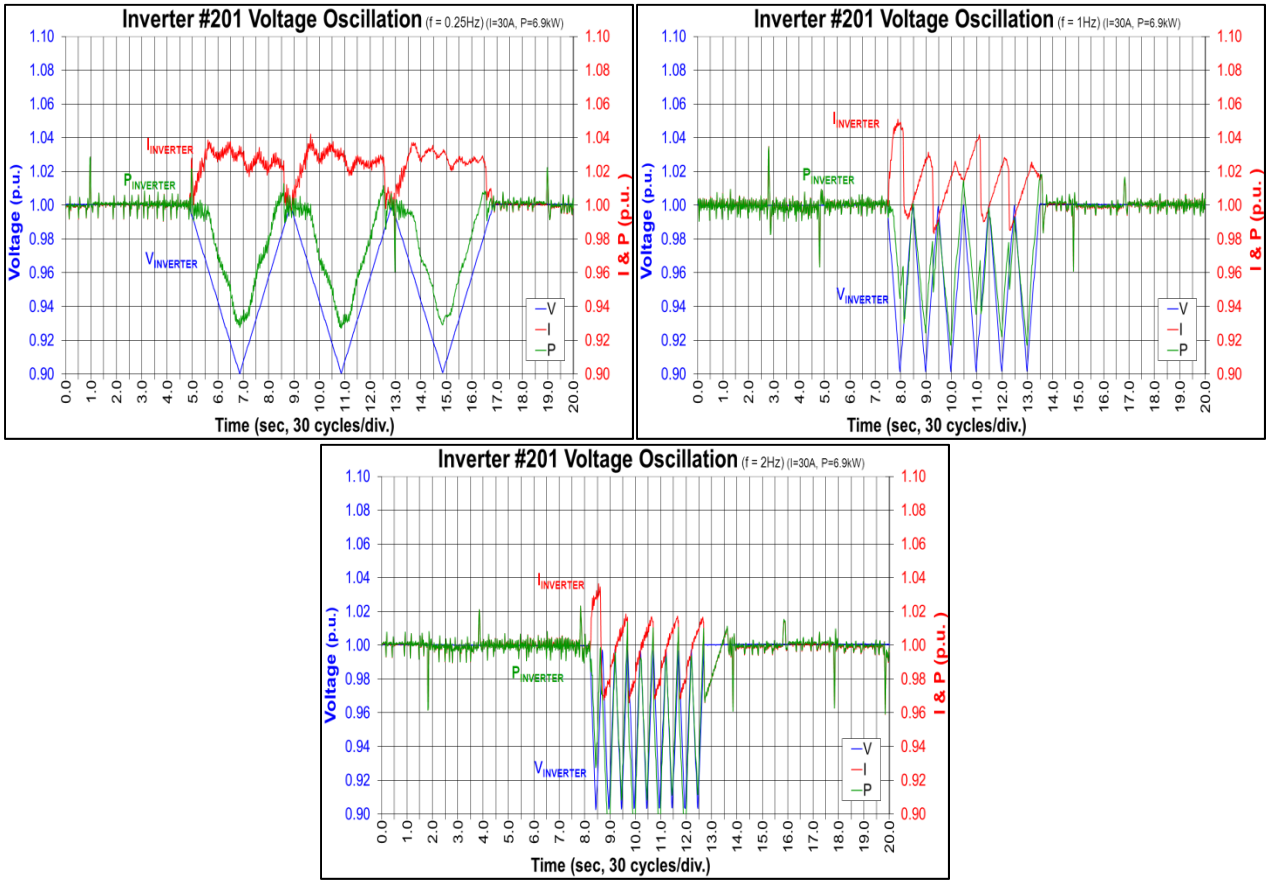

Figure 7.1.1 Voltage Oscillation Response (Inverter #201)

7.2 Inverter #202

The performance of Inverter 202 during voltage oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, and 2 Hz) is shown in Figure 7.2.1.

- Current responds quickly for all cases and isn't affected by the maximum output current limit (10%)
- Current oscillates opposite of voltage (10% above nominal) at swing frequency of 0.25 Hz to maintain constant active power (P)
- Current oscillates similarly during 1 Hz and 2 Hz oscillations but with slightly larger power deviations
- Largest deviation in active power (P) is still within 4% of nominal output

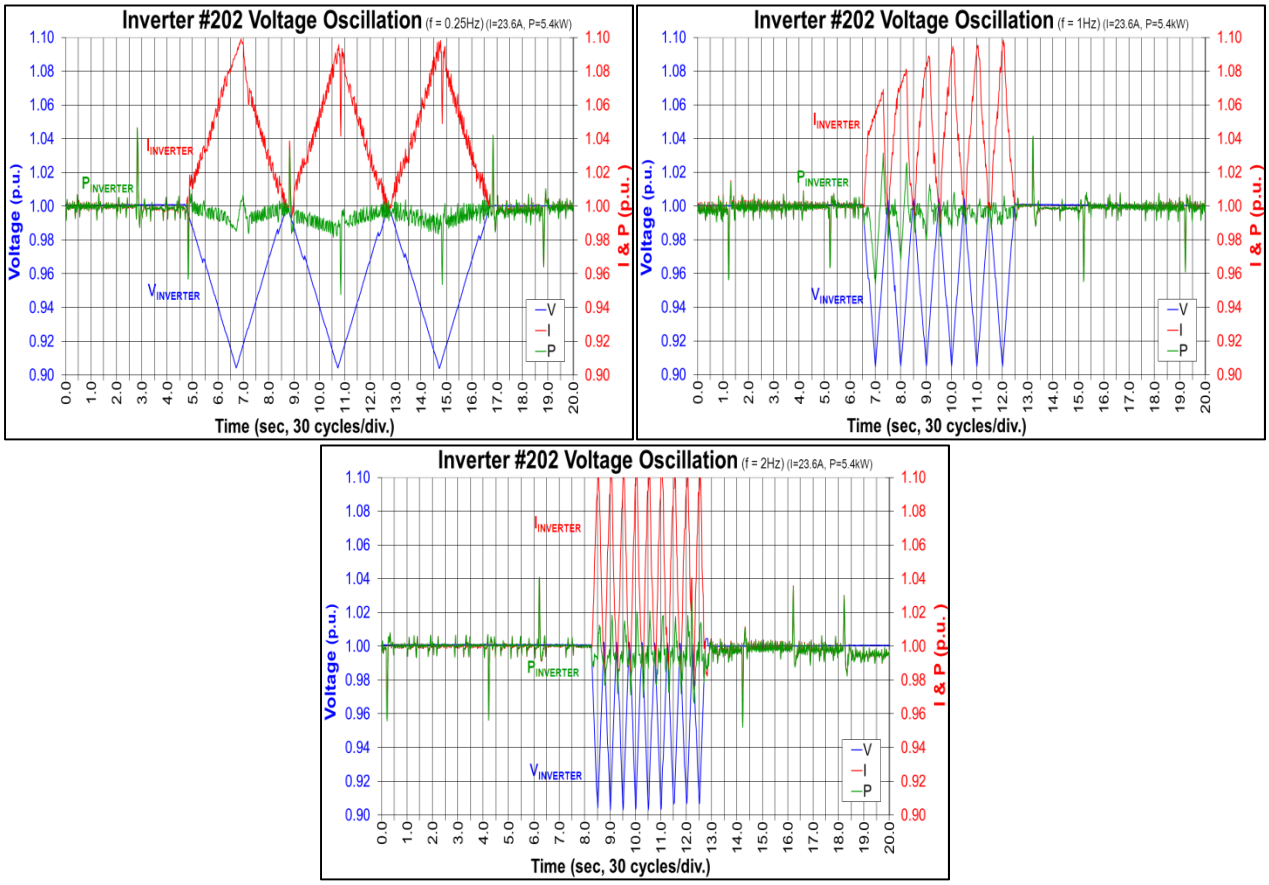

Figure 7.2.1 Voltage Oscillation Response (Inverter #202)

7.3 Inverter #203

Figure 7.3.1 below indicates the behavior for Inverter 203 during voltage oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, and 2 Hz).

- Current responds fastest during 0.25 Hz oscillations to minimize power oscillations (P deviates by 8%)
- Maximum current output limit (2% above nominal) prevents current from dampening power oscillations
- Larger power deviations (9%) occur during 1 Hz oscillations due to a slower current response
- Largest power deviations (11%) occur during 2 Hz oscillations from delayed current response

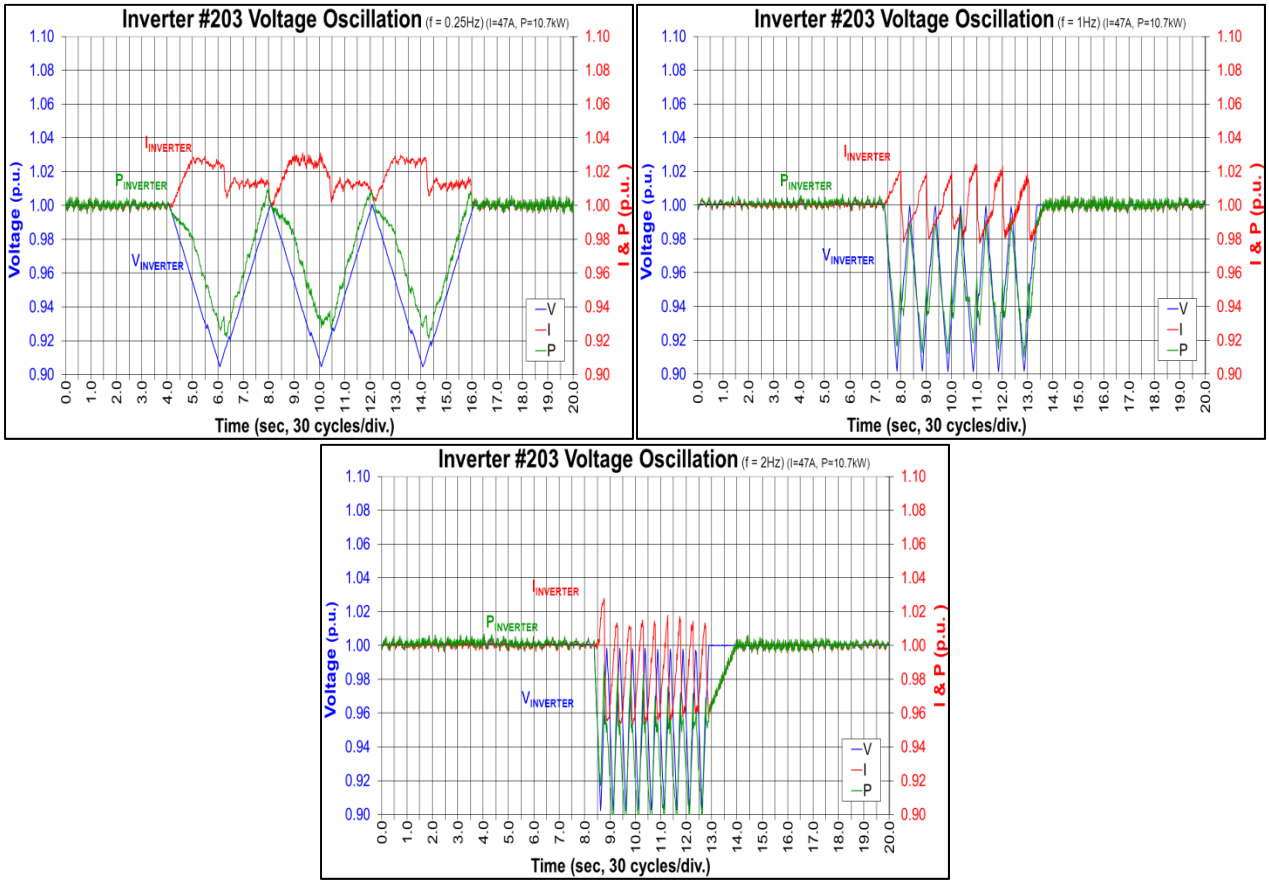

Figure 7.3.1 Voltage Oscillation Response (Inverter #203)

7.4 Inverter #205

The performance of Inverter 205 during voltage oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, and 2 Hz) is shown in Figure 7.4.1.

- Current responds quickly for all cases and is not affected by the maximum continuous output current limit
- Current oscillates opposite of voltage (12% above nominal) at swing frequency of 0.25 Hz to maintain constant active power (P)
- Current oscillates similarly but with distorted current profiles during 1 Hz and 2 Hz oscillations resulting in larger power deviations
- Largest deviation in active power (P) is within 8% of nominal output

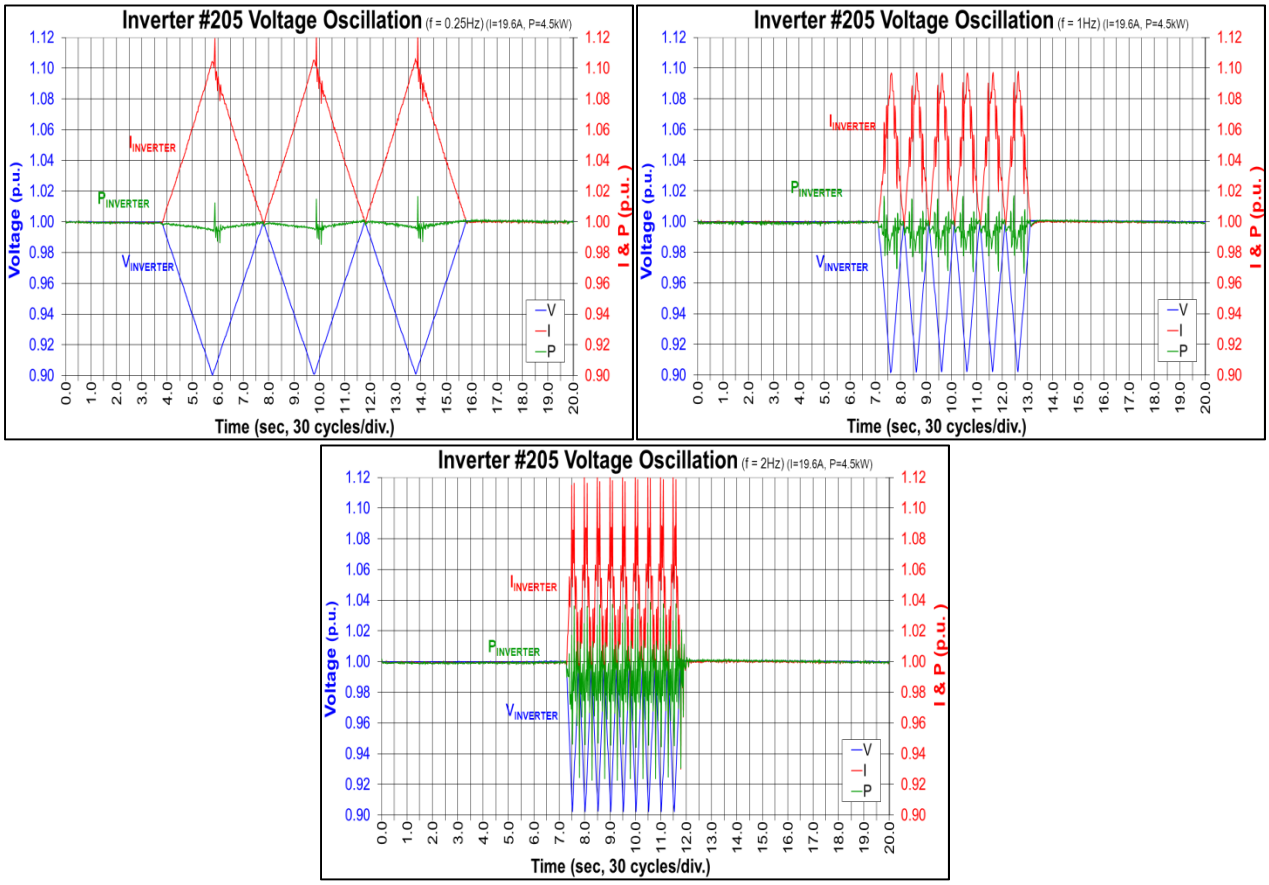

Figure 7.4.1 Voltage Oscillation Response (Inverter #205)

8.0 FREQUENCY OSCILLATION

The grid frequency was shifted between 59.4Hz and 60.4Hz to create frequency oscillations in order to assess the behavior of the inverters during these frequency variations. Frequency oscillations were performed at different rates, with swing frequencies of 0.25 Hz, 1 Hz, and 2 Hz. Table 8.0.1 shows the performance of all the inverters during frequency oscillations.

- All inverters trip off during 0.25 Hz and 1 Hz oscillations from frequency protection
- Negligible changes in current or active power output (all within 5% of nominal)
- Inverter 205 tripped off for every frequency oscillation test

Manuf. #	Inverter #	f_{swing}	$I_{DEVIATION}$ (± %)	$P_{DEVIATION}$ (± %)	Comments
4	201	0.25 Hz	NA	NA	Inverter Tripped Off
		1.0 Hz	NA	NA	Inverter Tripped Off
		2.0 Hz	5% ~ -1%	4% ~ -2%	Current and Power oscillate opp. of frequency during under-frequencies
	202	0.25 Hz	NA	NA	Inverter Tripped Off
		1.0 Hz	NA	NA	Inverter Tripped Off
		2.0 Hz	4% ~ -1%	2% ~ -1%	Current and Power oscillate opp. of frequency during under-frequencies
	203	0.25 Hz	NA	NA	Inverter Tripped Off
		1.0 Hz	NA	NA	Inverter Tripped Off
		2.0 Hz	1% ~ -1%	1% ~ -2%	Current and Power oscillate with the frequency (very small oscillations)
	205	0.25 Hz	NA	NA	Inverter Tripped Off
		0.25 Hz	NA	NA	Inverter Tripped Off
		0.25 Hz	NA	NA	Inverter Tripped Off

Table 8.0.1 Frequency Oscillation Response (f_{swing} = 0.25, 1.0, and 2.0 Hz)

8.1 Inverter #201

Figure 8.1.1 below indicates the behavior for Inverter 201 during frequency oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, 2 Hz).

- Frequency protection trips the inverter off during 0.25 Hz and 1 Hz oscillations
- Current oscillates opposite of frequency (as much as 5% above nominal) during 2 Hz oscillations
- Active power (P) is steadily deviating (as much as 4% above nominal)

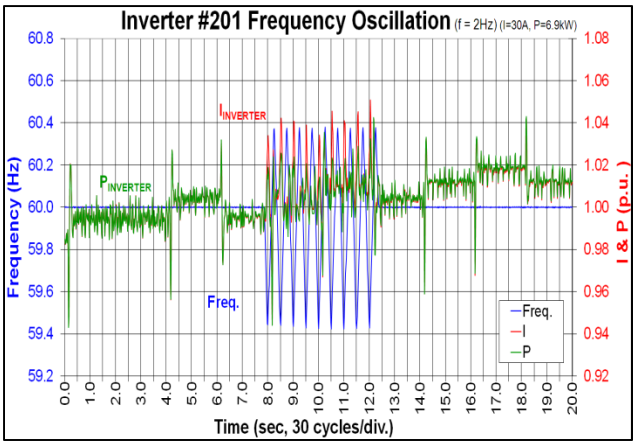

Figure 8.1.1 Frequency Oscillation Response (Inverter #201)

8.2 Inverter #202

The performance of Inverter 202 during frequency oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, 2 Hz) is shown in Figure 8.2.1 below.

- Frequency protection trips the inverter off during 0.25 Hz and 1 Hz oscillations
- Current oscillates opposite of frequency (as much as 4% above nominal) during 2 Hz oscillations
- Active power (P) oscillates with current (within 2% of nominal)

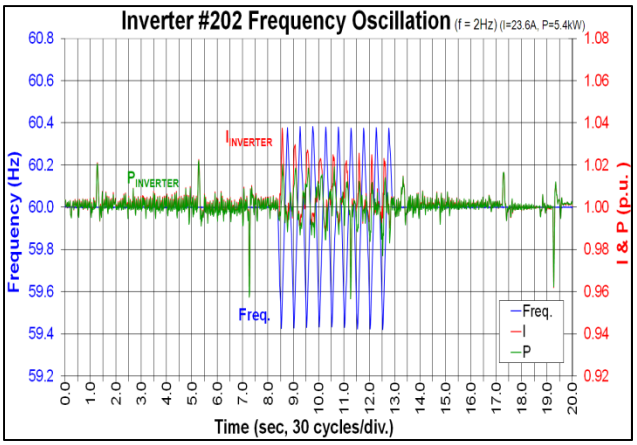

Figure 8.2.1 Frequency Oscillation Response (Inverter #202)

8.3 Inverter #203

Figure 8.3.1 below indicates the behavior for Inverter 203 during frequency oscillation tests at different swing frequencies (0.25 Hz, 1 Hz, 2 Hz).

- Frequency protection trips the inverter off during 0.25 Hz and 1 Hz oscillations
- A delayed response causes current to slightly oscillate with the system frequency (within 1% of nominal) during 2 Hz oscillations
- Active power (P) is also slightly deviating (within 2% of nominal)

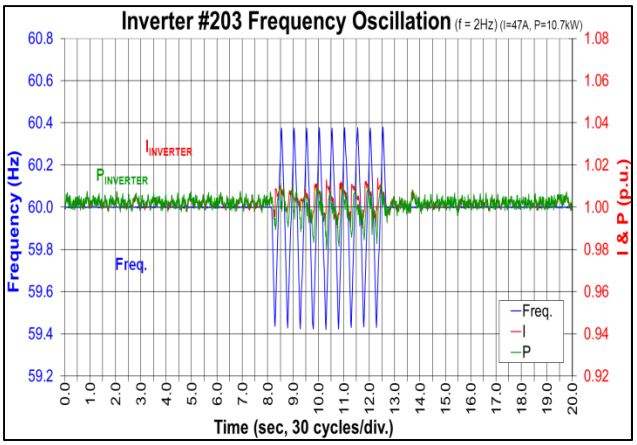

Figure 8.3.1 Frequency Oscillation Response (Inverter #203)

8.4 Inverter #205

Inverter 205 tripped of during frequency oscillation tests and could not be tested.

9.0 CONSERVATION VOLTAGE REDUCTION

The purpose of this test was to find out the inverter performance during conservation voltage reduction (CVR). The grid voltage was reduced from steady-state in increments of 1% to understand the inverters response and ability to maintain constant power over longer periods in the cases where the system undergoes conservation voltage reduction (CVR).

- Inverters 201 and 203 cannot maintain constant power once reaching their respective current output limits and therefore these devices will not maintain constant power during CVR
- Inverters 202 and 205 prevent real and reactive power reduction throughout the duration of the CVR test which is accomplished by injecting more current into the circuit
- Despite the inverter output current limits, all inverters provide enough current to support voltage drops when an increase in current is possible

9.1 Inverter #201

Figure 9.1.1 below indicates the behavior for Inverter 201 during the conservation voltage reduction test at unity and 0.9 power factors.

- Inverter maintains constant active power (P) until the maximum output current limit is reached
  - At 1.0 PF, current becomes clipped or limited at 3% above steady state
  - At 0.9 PF, current becomes clipped or limited at 2% above steady state
- Prior to the output current limit, current increases about 1% for 1% voltage decrement
- Active power (P) only drops as far as 2% below nominal power

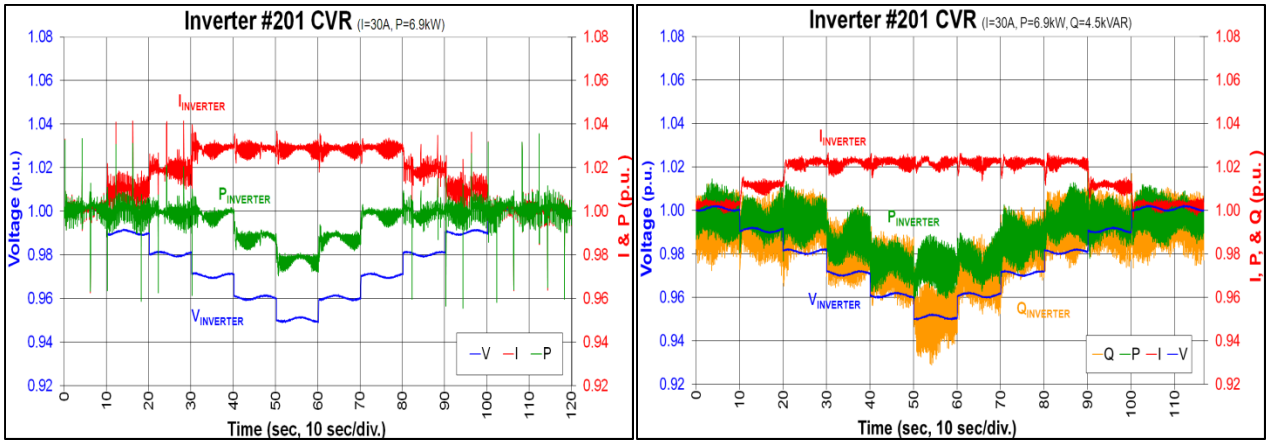

Figure 9.1.1. Conservation Voltage Reduction (Inverter #201; 1.0 PF and 0.9 PF)

9.2 Inverter #202

The behaviors of Inverter 202 during CVR tests at unity and 0.9 power factors are shown in Figure 9.2.1 below.

- Inverter prevents real (P) and reactive (Q) power loss during voltage reduction
- Current output responds quickly by increasing 1% for every 1% decrease in voltage

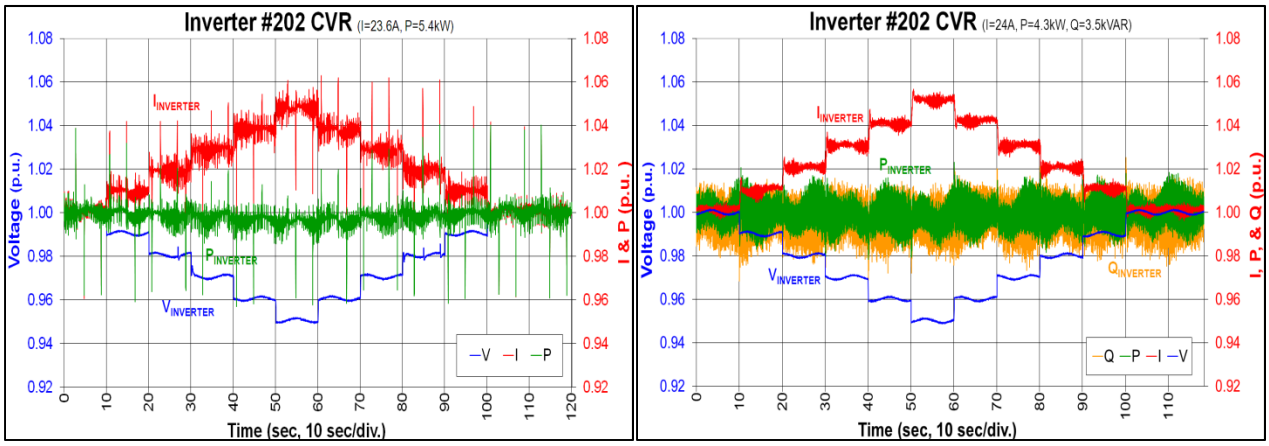

Figure 9.2.1. Conservation Voltage Reduction (Inverter #202; 1.0 PF and 0.9 PF)

9.3 Inverter #203

Figure 9.3.1 below indicates the behavior for Inverter 203 during the conservation voltage reduction test at unity and 0.9 power factors.

- Inverter maintains constant active power (P) until the maximum output current limit is reached
  - At 1.0 PF, current becomes clipped or limited at 2% above steady state
  - At 0.9 PF, current becomes clipped or limited at 1.7% above steady state
- Prior to the output current limit, current increases roughly by 1% for every 1% decrease in voltage
- Active power (P) only declines as far as 3% below nominal power

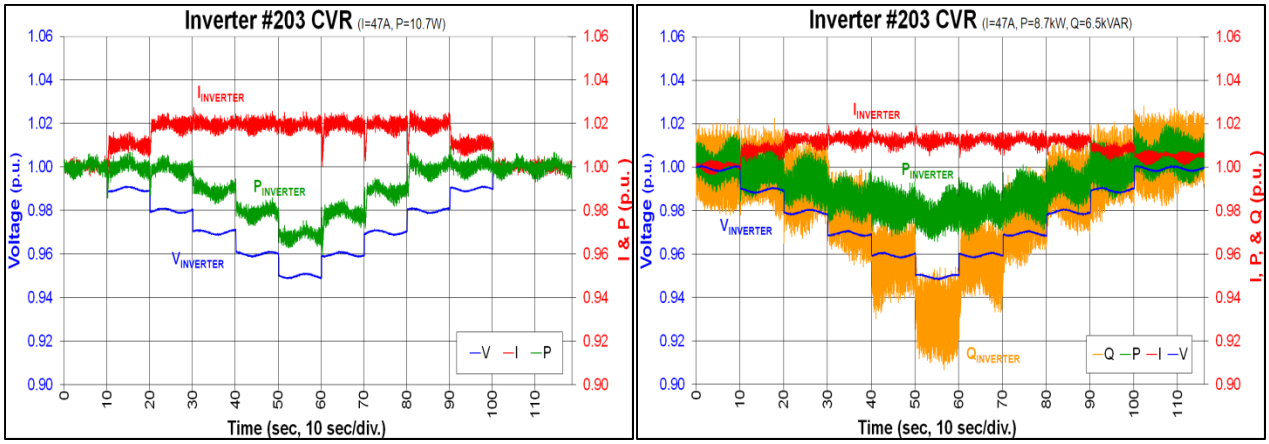

Figure 9.3.1. Conservation Voltage Reduction (Inverter #203; 1.0 PF and 0.9 PF)

9.4 Inverter #205

The behaviors of Inverter 205 during CVR tests at unity and 0.9 power factors are shown in Figure 9.4.1 below.

- Inverter prevents real (P) and reactive (Q) power loss during voltage reduction
- Current output responds quickly by increasing 1% for every 1% decrease in voltage

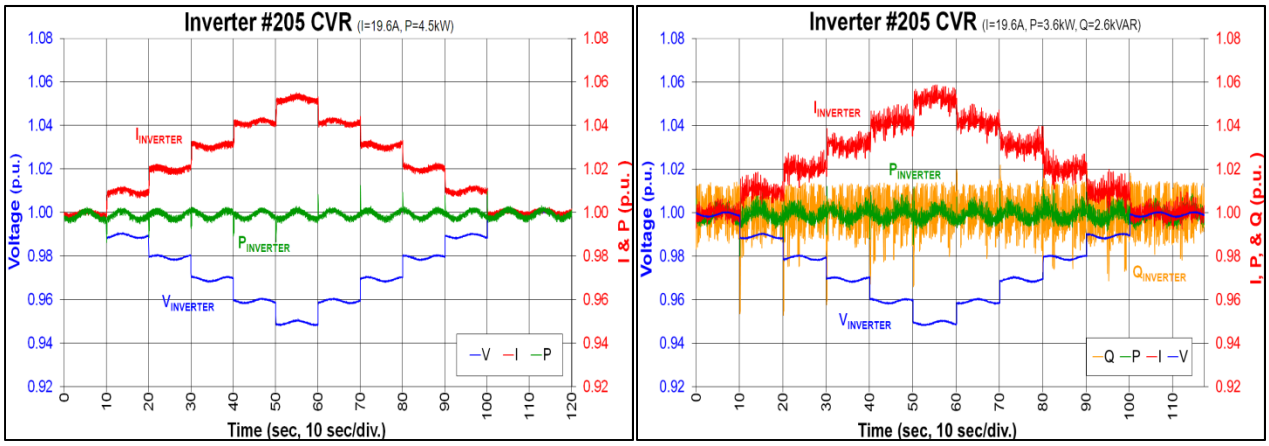

Figure 9.4.1. Conservation Voltage Reduction (Inverter #205; 1.0 PF and 0.9 PF)

ADVANCED FEATURES TESTING

10.0 START-UP POWER RAMP RATES

Each inverter was energized at the output AC terminals and then fed power into its DC terminals, with the PV simulator, in order to assess the inverter start-up behavior under a series of adjustable power ramp rates. This function can be used to slowly increase the inverters output power upon starting up or reconnection. The test results of the four tested inverters are shown in Figure 10.0.1.

Adjustable Settings:

- **WGra**: is the power ramp rate. It was set 1 to 1000% P_{MAX} per second; default 20% P_{MAX} per second

Tests performed:

- Slope A = 20% P_{MAX} per second (ramp duration of 5 seconds)
- Slope B = 2% P_{MAX} per second (ramp duration of 50 seconds)

Results:

- All inverters followed the expected slope behavior based on their setting
- No unexpected issues involving the system voltage upon start-up

Benefits:

- Mitigate distribution circuit voltage fluctuations during start-up conditions at high solar PV penetrations

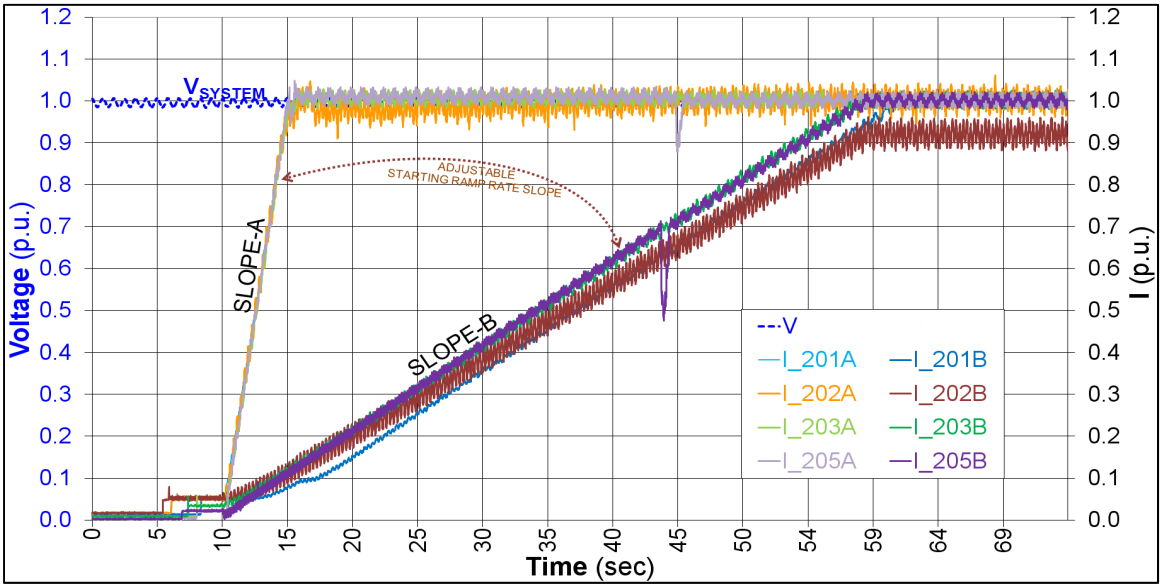

Figure 10.0.1 Adjustable Start-up Power Performance

11.0 LOW VOLTAGE RIDE THROUGH

The grid simulator voltage was programmed to follow a FIDVR event profile as shown in Figure 11.0.1 order to assess the inverters ride through behavior, specifically the response of the current and active power. Voltage falls to 45% and takes approximately 16 seconds to recover followed by a system over-voltage.

Adjustable Settings: are shown in Table 11.0.1 and Table 11.0.2

- Adjustable voltage protection thresholds and corresponding clearing times
  - **Vac-Min**: is the slow voltage protection set point
  - **Vac-Min-Tm**: is the timer for the slow voltage protection set point
  - **Vac-Min-Fast**: is the fast voltage protection set point
  - **Vac-Min-Fast-Tm**: is the timer for the fast voltage protection set point
- **DGS-PWMVolNom**: is the Low Voltage Threshold. The inverter will cease generating power to the grid when voltage falls below this value
- **DGS-HystVolNom**: is the restart Hysteresis. The inverter begins generating again when voltage exceeds the sum of this value and the cease generation voltage threshold

Tests Performed:

- LVRT during FIDVR event without triggering cease generation feature (passive)
- LVRT during FIDVR event using cease generation feature (active)

Benefits:

- Support the grid during contingencies such as FIDVR events and prevent unnecessary tripping for large penetrations of solar PV generation

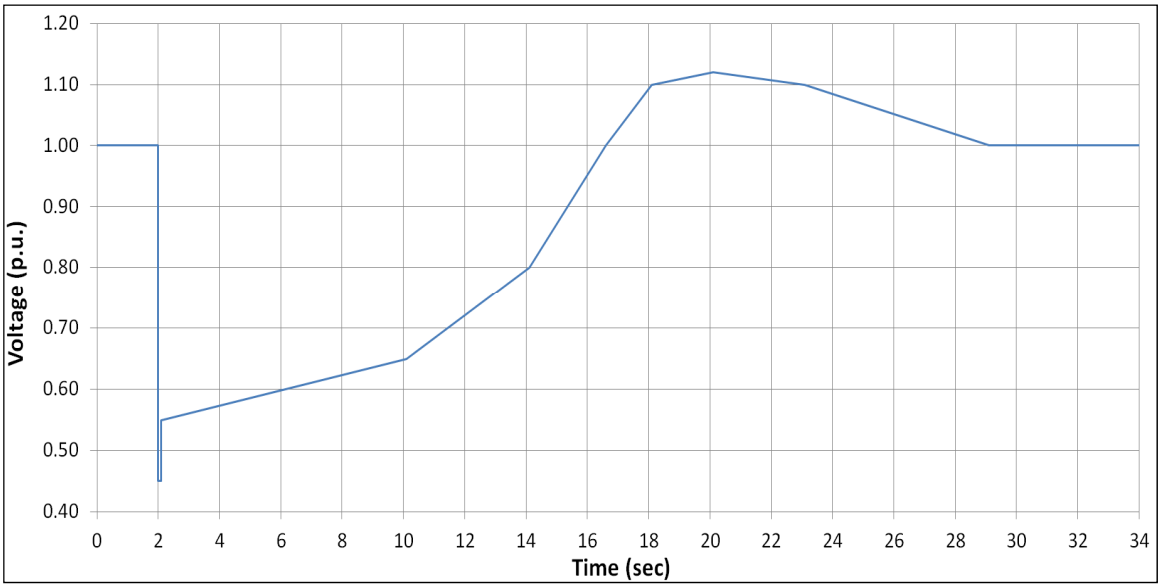

Figure 11.0.1 FIDVR Profile

Name	Min. Value	Max. Value	Default Value	Unit
Vac-Max-Fast	100	300	-	V
Vac-Max-Fast-Tm	0.04	60	-	s
Vac-Max	100	300	-	V
Vac-Max-Tm	0.04	60	-	s
Vac-Min	70	230	-	V
Vac-Min-Tm	0.04	10	-	s
Vac-Min-Fast	70	230	-	V
Vac-Min-Fast-Tm	0.04	10	-	s
DGS-HystVolNom	0	60	5	%
DGS-PWMVolNom	40	100	70	%

Table 11.0.1 Voltage Protection Parameters (Inverter #201 – #204)

One of the inverters had different names and additional protection settings, as shown in Table 11.0.2.

- **VolCtl.hhLim**: is the fast high voltage protection set point
- **VolCtl.hhLimTms**: is the timer for the fast high voltage protection set point
- **VolCtl.hLim**: is the slow high voltage protection set point
- **VolCtl.hLimTms**: is the timer for the slow high voltage protection set point
- **VolCtl.lLim**: is the fast low voltage protection set point
- **VolCtl.lLimTms**: is the timer for the fast low voltage protection set point
- **VolCtl.llLim**: is the slow low voltage protection set point
- **VolCtl.llLimTms**: is the timer for the slow low voltage protection set point
- **DGS-PWMVolNom**: is the Low Voltage Threshold. The inverter will cease generating power to the grid when voltage falls below this value
- **DGS-HystVolNom**: is the restart Hysteresis. The inverter begins generating again when voltage exceeds the sum of this value and the cease generation voltage threshold

Name	Min. Value	Max. Value	Default Value	Unit
VolCtl.hhLim	100	300	-	V
VolCtl.hhLimTms	0	60000	-	ms
VolCtl.hLim	100	280	-	V
VolCtl.hLimTms	0	60000	-	ms
VolCtl.lLim	45	230	-	V
VolCtl.lLimTms	0	10000	-	ms
VolCtl.llLim	45	230	-	V
VolCtl.llLimTms	0	10000	-	ms
DGS-HystVolNom	0	100	5	%
DGS-PWMVolNom	0	100	70	%

Table 11.0.2 Voltage Protection Parameters (Inverter #205)

11.1 LVRT when Voltage above Threshold

Figure 11.1.1 below indicates the inverters behavior during a FIDVR event when the voltage is not low enough (above this setting **"DGS-PWMVolNom"**) for the inverters to cease generating power into the grid.

Test Settings:

- Low Voltage Threshold = 40%
- Restart Hysteresis = 5%

Test Results:

- Inverters stay online and continue generating power for the entire FIDVR event
- During under-voltage condition, inverters produce maximum output current to support generation
  - Inverter 201 current clipped at 3% above nominal
  - Inverter 202 current clipped at 10% above nominal
  - Inverter 203 current clipped at 2% above nominal
  - Inverter 205 current clipped at 11% above nominal
- During over-voltage condition, all inverters reduce current output to maintain constant power

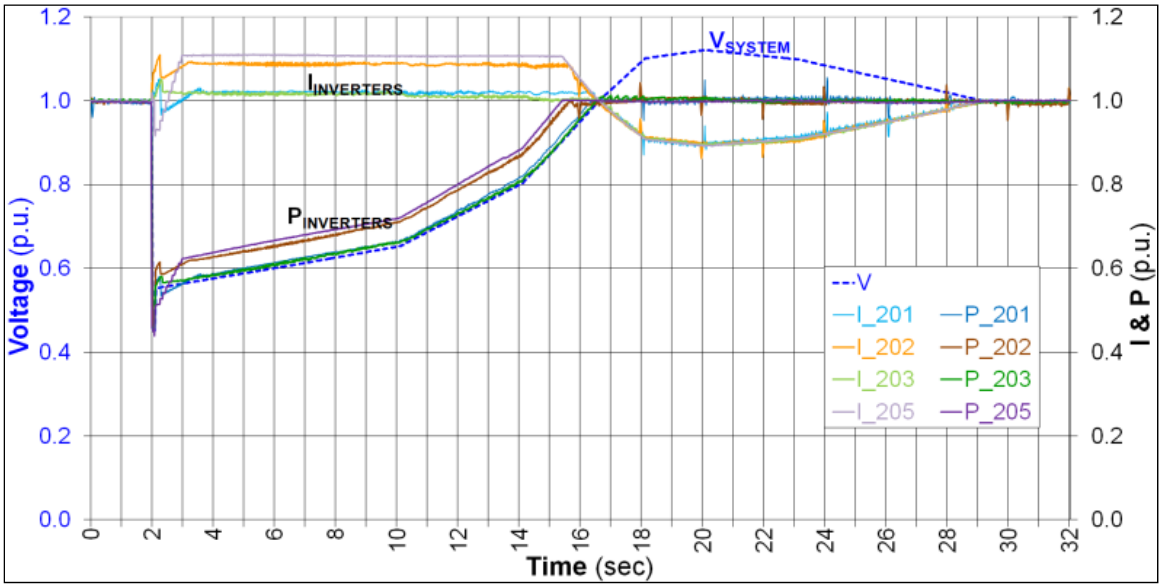

Figure 11.1.1 Passive LVRT Performance

11.2 LVRT when Voltage below Threshold

Figure 11.2.1 below indicates the inverters behavior during a FIDVR event when the voltage is too low (below this setting **"DGS-PWMVolNom"**) and the inverters cease generating power into the grid until the voltage goes above the programmed threshold.

Test Settings:

- Low Voltage Threshold = 47%
- Restart Hysteresis = 3%

Test Results:

- Inverters stop generating power once voltage falls below 47% and begin generating again at (47%+3%) 50% voltage (in first 6 cycles of the FIDVR event shown)
- Current ramps up to steady state according to the adjustable ramp rate (**"WGra"**) from Section 10.0
    - Ramp rates > 150% P_{MAX} per second result in instantaneous over-current (110%-135% nominal)
- The inverters will generate the maximum current available if there is still an under-voltage
- During an over-voltage condition, the inverters reduce current output to maintain constant power

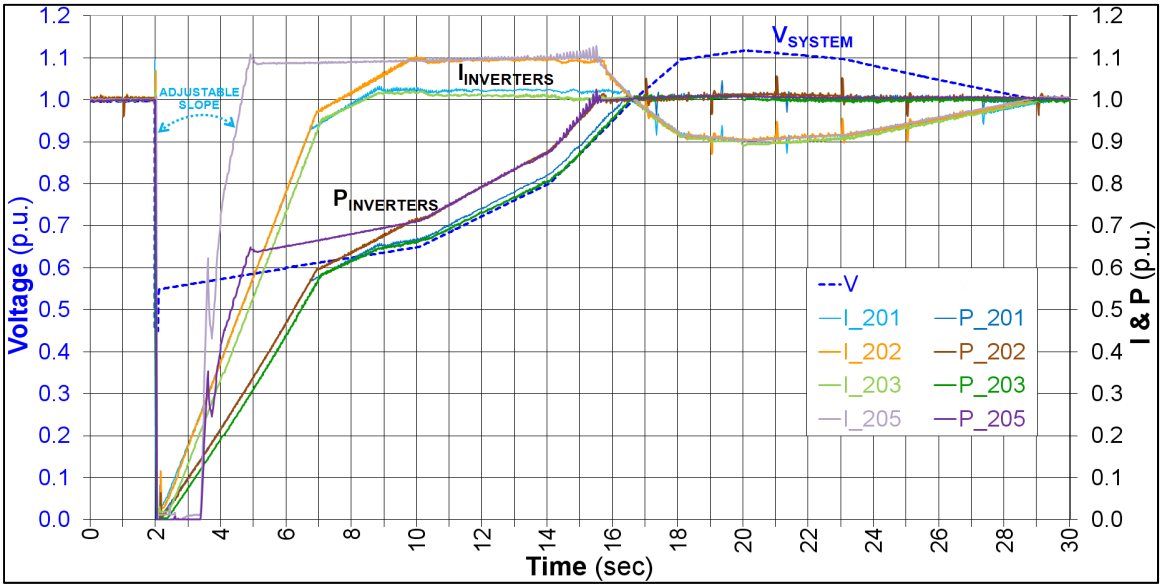

Figure 11.2.1 Active LVRT Performance

12.0 POWER CURTAILMENT

The grid frequency was ramped up and down while maintaining constant load in order to assess the inverters power reduction behavior during over-frequency conditions. Over-frequency conditions are typically produced during instances of over-generation on a circuit.

Adjustable Settings: are shown in Table 12.0.1

- **P-HzStr**: is the over-frequency threshold. The inverter limits its output power when frequency goes above this value
- **P-WGra**: is the power limit slope. Defines the relationship between the active power limitation and over-frequency values
- **P-HystEna**: It is the power limit at maximum over-frequency. The inverter continuously limits its output power during the maximum over-frequency condition until being reset
- **P-HzStop**: is the power-reset frequency threshold. The power output resets when frequency falls below this value
- **P-HzStopWGra**: is the power-reset ramp rate. Is the speed at which power recovers to nominal after being reset

Tests Performed:

- **P-HystEna**: is the over-frequency ramp. For these tests it was disabled (Linear Power Curtailment with Over-frequency)
- **P-HystEna**: is the over- frequency ramp. For these tests it was enabled (Constant Power Curtailment at Max Over-frequency)

Benefits:

- Prevent unnecessary tripping of generation during over-frequency events
- Support the system during cases of over-generation

Name	Min. Value	Max. Value	Default Value	Unit
P-HzStr	0	5	0.2	Hz
P-WGra	10	130	40	%/Hz
P-HystEna	Off	On	Off	
P-HzStop	0	5	0.2/0.05	Hz
P-HzStopWGra	1	10000	10000	%/min

Table 12.0.1 Power Curtailment Parameters

12.1 Linear Power Curtailment with Over-frequency

Figure 12.1.1 below indicates the inverters' behavior during a frequency ramp where the power limitation has a linear relationship with over-frequency.

Test Settings:

- Over-frequency Threshold = 60.2 Hz
- Power Limit Slope = 50% P_{MAX} / Hz
- Power Limit at Max. Over-frequency = Off

Test Results (See Figure Below):

- Power begins ramping down, shortly after the system frequency goes above the 60.2 set threshold, according to the limit slope (reduces power by 50% for every increase of 1 Hz)
- Active power also begins ramping up as system frequency returns to steady state (60Hz)
    - For 61 Hz over-frequency ramp, some inverters experience different delays in performance as power recovers/ramps up
    - For 60.6 Hz over-frequency ramp, there are no delays as power recovers/ramps up

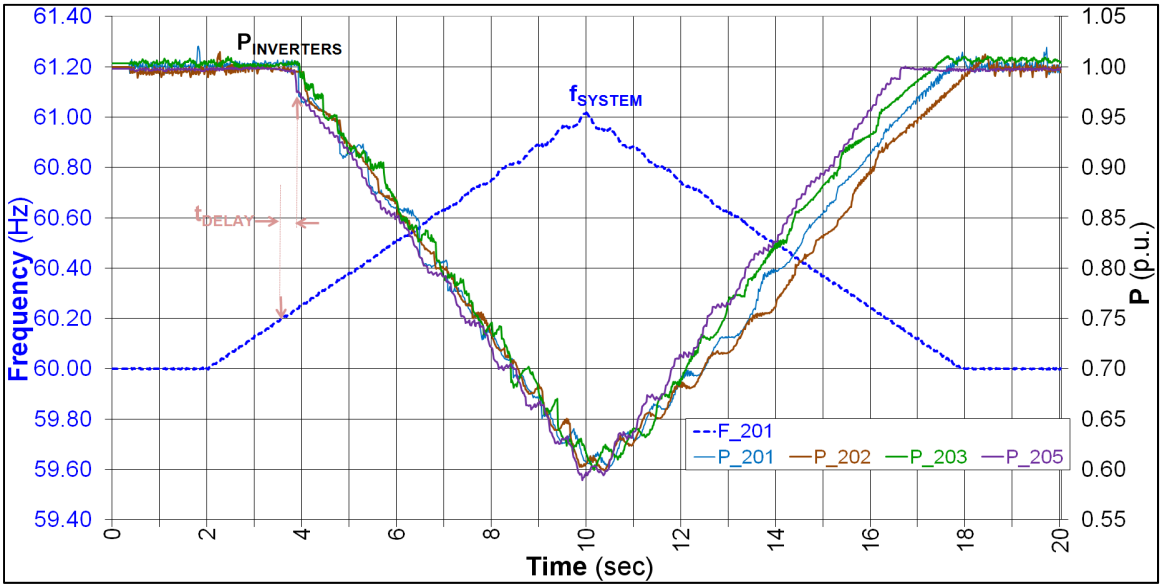

Figure 12.1.1 Linear Power Curtailment with Over-frequency Performance

12.2 Constant Power Curtailment at Max Over-frequency

Figure 12.2.1 below indicates the inverters behavior over-frequency event when the power limit at maximum over-frequency feature is enabled.

Test Settings:

- Over- frequency Threshold = 60.2 Hz
- Power Limit Slope = 50% PMAX / Hz
- Power Limit at Max. Over-frequency = On
- Power-Reset Frequency Threshold = 60.2 Hz
- Power-Reset Ramp Rate = 10,000% PMAX / min

Test Results:

- Power begins ramping down, shortly after the system frequency goes above the threshold, according to the limit slope (reduces power by 10% for every increase of 0.2 Hz)
- Once the active power reaches 60% (at max over-frequency), it is limited at this value no matter if the frequency value goes down until the frequency falls below the programmed threshold
- Power immediately ramps up to steady state after being reset when frequency falls below 60.2 Hz

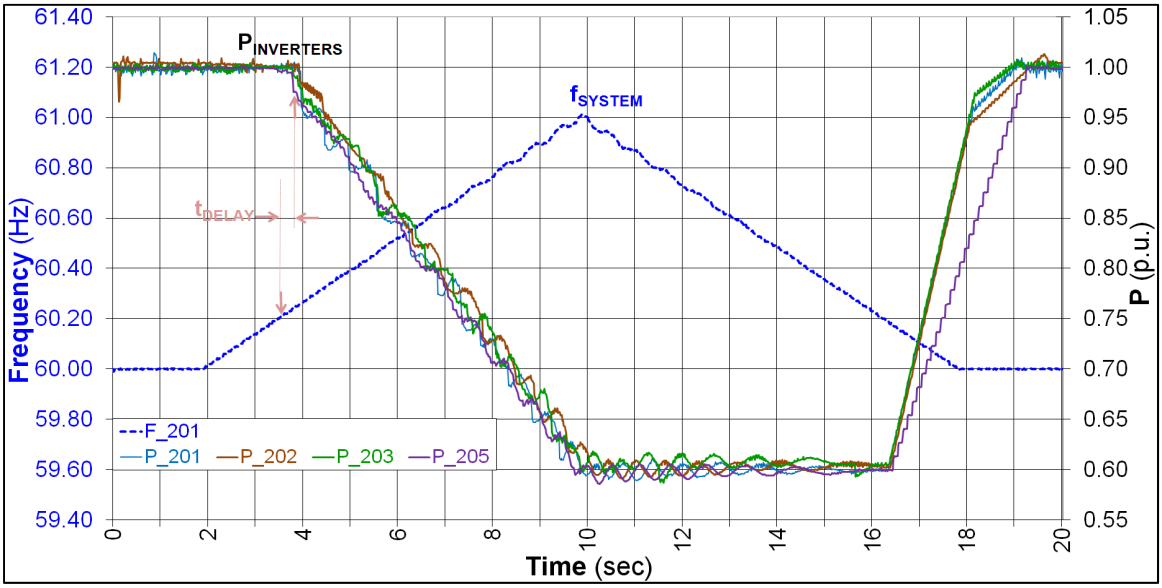

Figure 12.2.1 Constant Power Curtailment at Max Over-frequency Performance

13.0 AUTONOMOUS VOLTAGE SUPPORT (POWER FACTOR ADJUSTMENT)

This inverter can be set to provide leading, lagging, or unity power factor at low generation (typically morning or afternoon) and dynamically adjust its power factor through the day based on its power output. In order to simulate this in the laboratory, the PV simulator was programmed to ramp up its power output in order to assess the inverters ability to autonomously adjust its power factor as shown in Figure 13.0.1. PV simulator's irradiance setting was programmed to ramp from 60% to 100%.

Adjustable Settings: are shown in Table 13.0.1

- **PF-WNomStr**: is the active power start point. The inverter linearly adjusts PF when power goes above this value
- **PF-PFStr**: is the PF start point. The inverter PF when output power ≤ "Active Power Start Point"
- **PF-PFExtStr**: is the excitation start point. The excitation type of "PF Start Point", either leading or lagging
- **PF-WNomStop**: is the active power stop point. The inverter linearly adjusts PF when power goes below this value
- **PF-PFStop**: is the PF stop point. The inverter PF when output power ≥ "Active Power Stop Point"
- **PF-PFExtStop**: Excitation stop point. The excitation type of "PF Stop Point", either leading or lagging

Tests Performed:

- Ramp up PV simulator irradiance with PF set to change from unity to leading/lagging
- Ramp up PV simulator irradiance with PF set to change from leading/lagging to unity

Benefits:

- Feature could be used to implement power factor scheduling to provide local voltage support to distribution circuits with large penetrations of solar PV generation

Name	Min. Value	Max. Value	Default Value	Unit
PF-WNomStr	0	100	50	%
PF-PFStr	0.8	1	1	
PF-PFExtStr	Underexcited	Overexcited	Overexcited	
PF-WNomStop	0	100	100	%
PF-PFStop	0.8	1	1/0.95/0.9	
PF-PFExtStop	Underexcited	Overexcited	Underexcited	

Table 13.0.1 Autonomous Power Factor Parameters

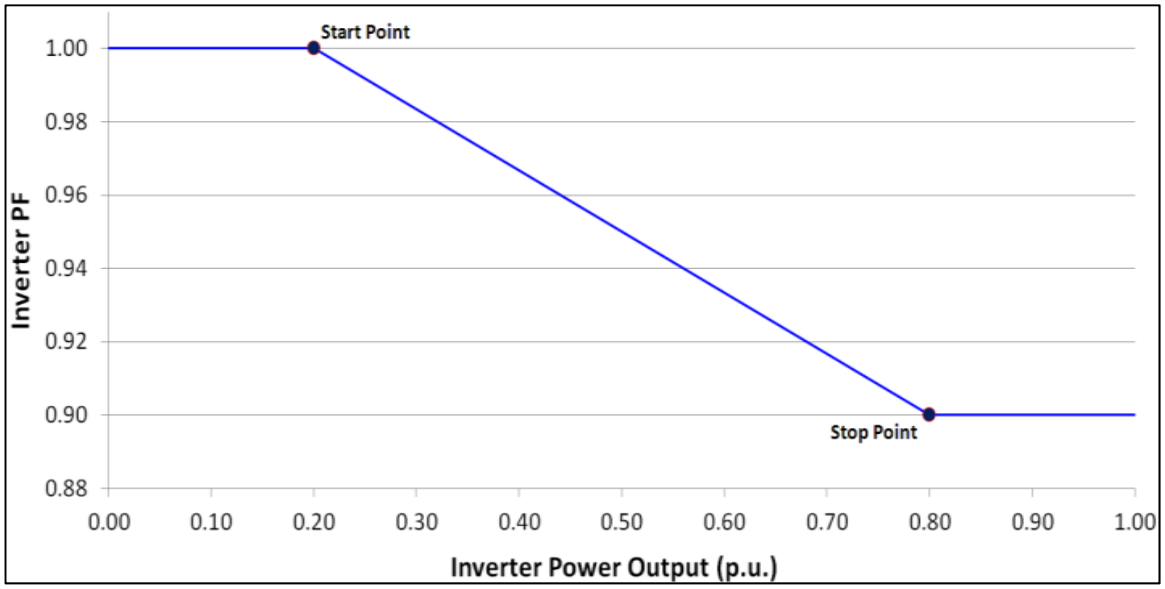

Figure 13.0.1 Sample Autonomous Power Factor Setup

13.1 Unity PF to Leading/Lagging PF

Figure 13.1.1 below shows the inverters autonomous power factor performance as generation increases. This test is to show that the inverter can start unity PF when the generation is at 70% or below and dynamically adjust its PF to either leading or lagging when the output power increases. This can provide voltage support to the distribution circuits by boosting or reducing the voltage depending on the needs of a particular circuit.

Test Settings:

- Active Power Start Point = 70%
- PF Start Point = 1.0
- Excitation Start Point = Overexcited (irrelevant at unity PF)
- Active Power Stop Point = 90%
- PF Stop Point = 0.9
- Excitation Stop Point = Underexcited/Overexcited

Test Results:

- Inverter initially operates at unity PF until real power output goes above 70% of nominal
- Power factor linearly ramps down to approximately 0.9 leading/lagging
- Inverter continues operating at 0.9 leading/lagging after it goes above 90% of nominal
- Some inverters ramp slightly slower/faster than others despite the exact same settings

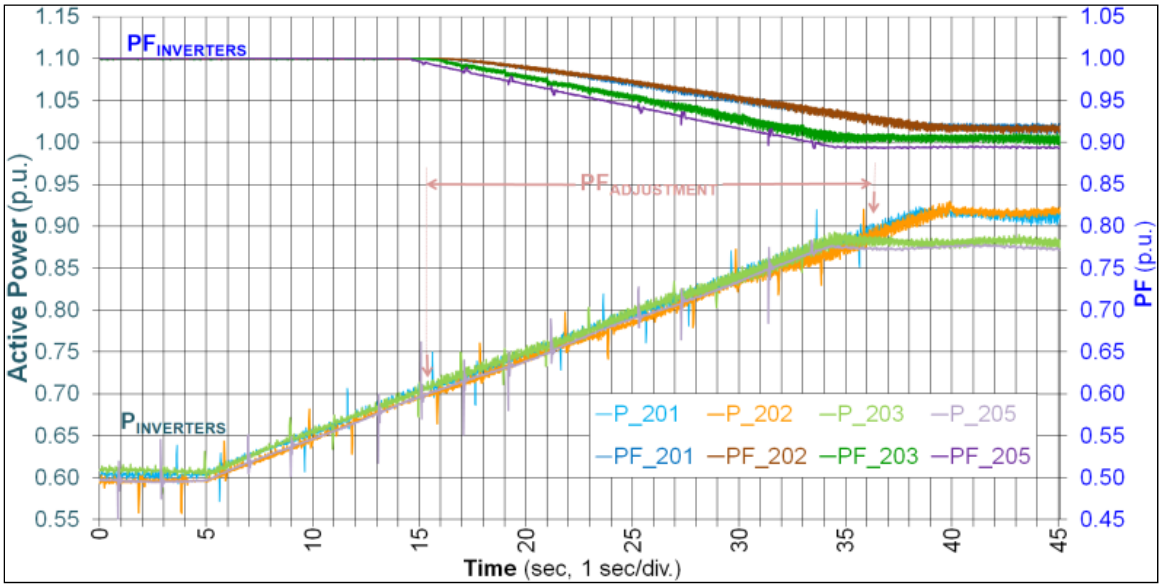

Figure 13.1.1 Unity PF to Leading/Lagging PF Performance

13.2 Leading/Lagging PF to Unity PF

Figure 13.2.1 below indicates the inverters autonomous power factor performance as generation increases. This test is to show that the inverter can start either leading or lagging when the generation is at 70% or below and dynamically adjust its PF to unity when the output power increases. This can provide voltage support to the distribution circuits by boosting or reducing the voltage depending on the needs of a particular circuit.

Test Settings:

- Active Power Start Point = 70%
- PF Start Point = 0.9
- Excitation Start Point = Underexcited/Overexcited
- Active Power Stop Point = 90%
- PF Stop Point = 1.0
- Excitation Stop Point = Overexcited (irrelevant at unity PF)

Test Results:

- Inverter initially operates at 0.9 power factor until generation increases above 70% of nominal
- Power factor linearly ramps up to unity when generation is above 70% of nominal
- Inverter continues operating at unity PF while generation is above 90% of nominal
- Some inverters ramp slightly slower/faster than others despite the exact same settings

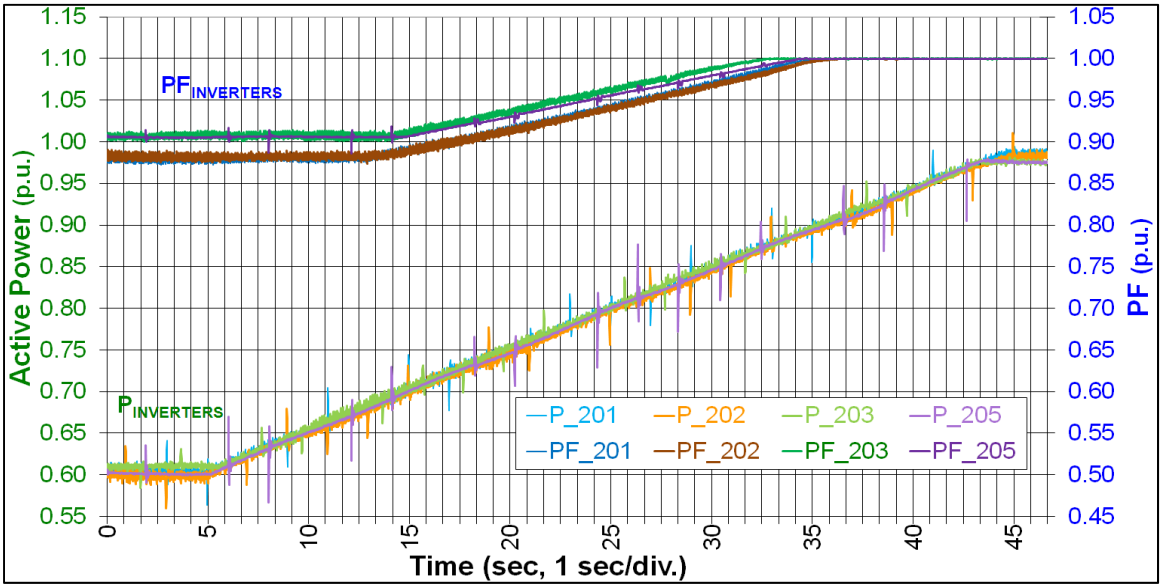

Figure 13.2.1 Leading/Lagging PF to Unity PF Performance

14.0 AUTONOMOUS VOLTAGE (VAR) SUPPORT

The grid simulator was programmed as a weak source where its output current was manually limited in approximately 5 second intervals. This system current limitation (weak source) will adjust the test setup generation-to-load ratio to either sag or swell the system voltage in order to assess the inverters voltage support functions.

Adjustable Settings: are shown in Table 14.0.1

- **Q-VArMaxNom**: is the maximum Q limit. The maximum amount of reactive power that can be provided, percentage is based on the inverters nominal power rating or P_{MAX}
- **Q-VArGraNom**: is the Q/V gradient. The slope of reactive power/voltage characteristic curve
- **Q-VArTms**: is the adjustment time. The adjustment time for the operating point of the characteristic curve
- **Q-VolWidNom**: voltage spread. The voltage region where voltage support is disabled (±X% voltage deviation)

Tests Performed:

- System voltage lowered in steps for multiple Volt/VAR feature settings
- System voltage increased in steps for multiple Volt/VAR feature settings

Benefits:

- Support the voltage (boost or buck) autonomously by injecting or absorbing reactive power

Name	Min. Value	Max. Value	Default Value	Unit
Q-VArMaxNom	0	50	0	%
Q-VArGraNom	0	10	0	%
Q-VArTms	2	60	10	s
Q-VolWidNom	0	20	0	%

Table 14.0.1 Voltage Support Parameters

14.1 Voltage/VAR Support During Under-voltage

Figure 14.1.1 below shows the inverters behavior with and without the autonomous voltage support feature enabled. At steady state voltage, the grid simulator's current was limited in 5 second intervals. By decreasing the setup's generation-to-load ratio, the system voltage sags as a result.

Test Settings:

- Maximum Q Limit = 50%
- Q/V Gradient = 0%, 1%, 3%
- Adjustment Time = 2 seconds
- Voltage Spread = 0%

Test Results:

- When the Volt/VAR feature is off, the inverter does not inject any VARs into the system
  - Voltage is ultimately depressed down to 81% of nominal
- When the Volt/VAR feature is on, the inverter increases its VAR output shortly after voltage drops below 98% of nominal and boosts the system voltage accordingly.
  - At Q/V = 1%, the inverter prevents voltage from falling below 89% of nominal
  - At Q/V = 3%, the inverter prevents voltage from falling below 91% of nominal

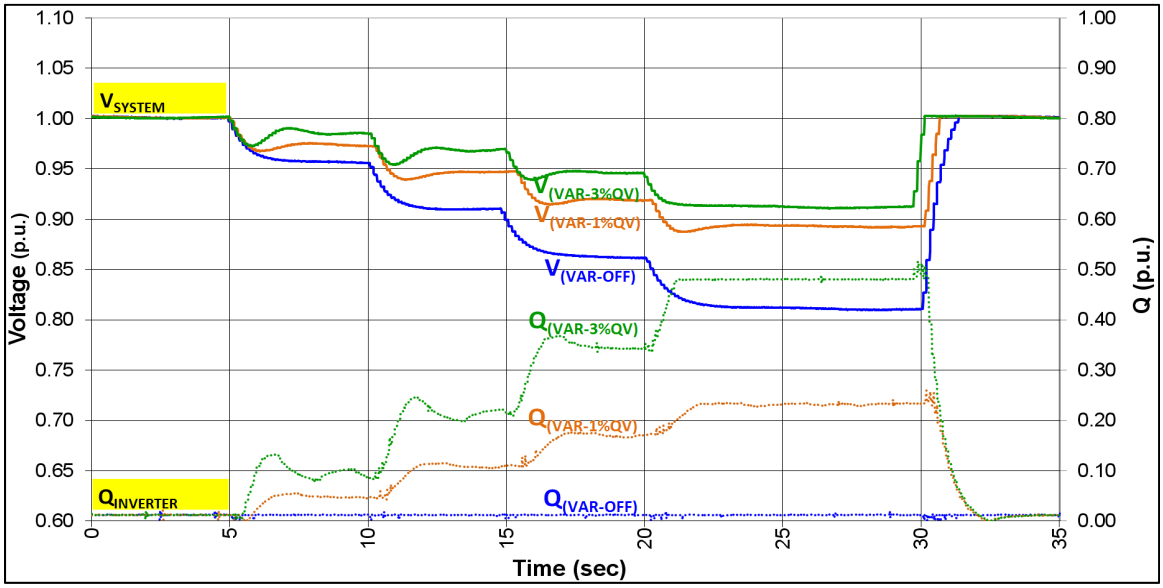

Figure 14.1.1 Voltage Support During Under-voltage

14.2 Voltage/VAR Support During Over-voltage

Figure 14.2.1 below shows the inverters behavior with and without the autonomous voltage support feature enabled. At steady state voltage, the grid simulator's current limit is increased in 5 second intervals. By increasing the setup's generation-to-load ratio, the system voltage swells as a result.

Test Settings:

- Maximum Q Limit = 50%
- Q/V Gradient = 0%, 1%, 3%
- Adjustment Time = 2 seconds
- Voltage Spread = 0%

Test Results:

- When the Volt/VAR feature is off, the inverter does not absorb any VARs from the system
  - Voltage is ultimately increased up to 120% of nominal
- When the Volt/VAR feature is on, the inverter begins drawing VARs shortly after voltage goes above 102% of nominal and bucks the system voltage accordingly.
  - At Q/V = 1%, the inverter prevents voltage from operating above 112% of nominal
  - At Q/V = 3%, the inverter prevents voltage from operating above 106% of nominal

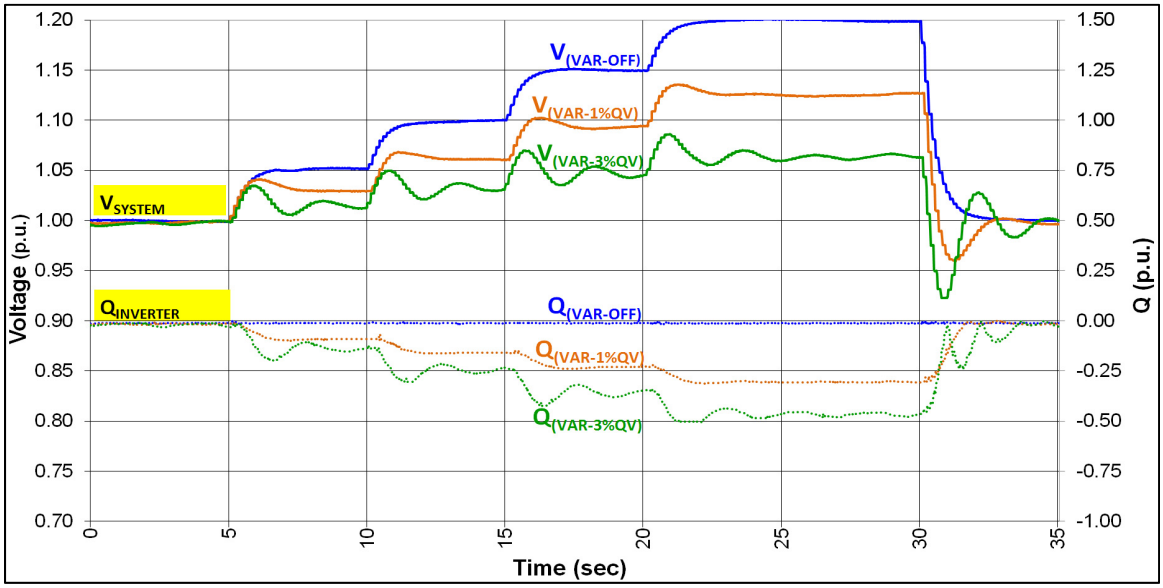

Figure 14.2.1 Voltage Support During Over-voltage

15.0 ISLANDING POTENTIAL (SINGLE INVERTER)

There is a concern that inverter advanced features may compromise the device's anti-islanding protection. This concern is shared by many utilities that want to ensure the safety of field personnel by preventing self-sustaining islands from occurring on the grid. The following test results are for Inverter 205 which is the only one of these tested inverters with Volt/VAR controls.

15.1 Islanding Potential with Adjusted Protection Settings

This inverter has a remote possibility of being islanded if someone were to enter wrong settings. All of the following settings must be changed in order for the inverter to remain generating power:

- wider frequency protection beyond IEEE 1547
- automatic match of load and generation
- anti-islanding protection disabled
- volt/var feature disabled

The inverter was islanded indefinitely and at least the first hour of islanding condition was recorded as shown in Figure 15.1.1.

Island Settings:

- Disabled the inverters anti-islanding detection setting ("Escalation factor")
- Real and reactive load reasonably matched inverter generation
- Under-frequency protection was set low (< 50 Hz)
- Disabled inverter volt/var control features

Test Results:

- Inverter immediately begins operating at approximately 54 Hz while successfully islanded
  - U.S. frequency protection standards would have resulted in the inverter tripping
- With constant load, inverter remains islanded for over an hour
- A static PF of 0.9 leading was used to maintain consistent generation values
  - Previous attempts with dynamic generation settings (i.e. Volt/VAR controls) resulted in tripping

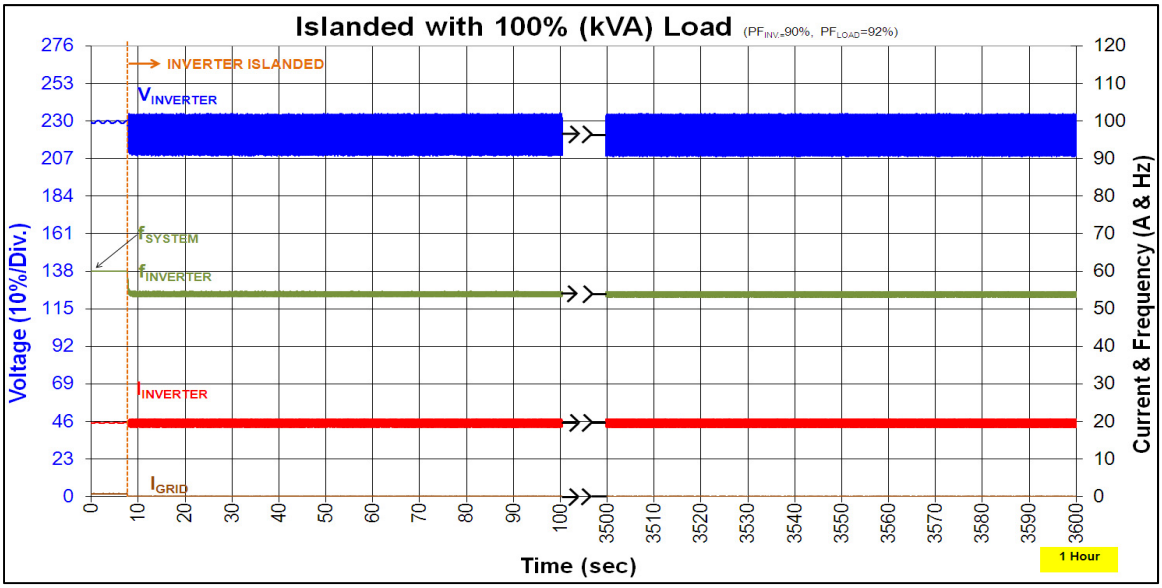

Figure 15.1.1 Inverter Islanded

15.2 Islanding Potential with Volt/VAR Controls

One of the concerns regarding smart inverters is whether or not the volt/var features will be able to override the anti-islanding protection allowing the device to continue operating off-grid. Therefore, the residential inverter was disconnected from the grid with matched load to evaluate its performance. The tests conducted reveal no evidence that the inverters volt/var features will result in an islanded condition.

Island Settings #1:

- Enabled inverter volt/var control features
- Real and reactive load reasonably matched inverter generation

Test Results #1: are shown in Figure 15.2.1

- Inverter begins drifting out of phase immediately after grid disconnection
- Voltages fluctuate as high as 113% nominal voltage
- Inverter shuts down within 6.5 cycles after being disconnected

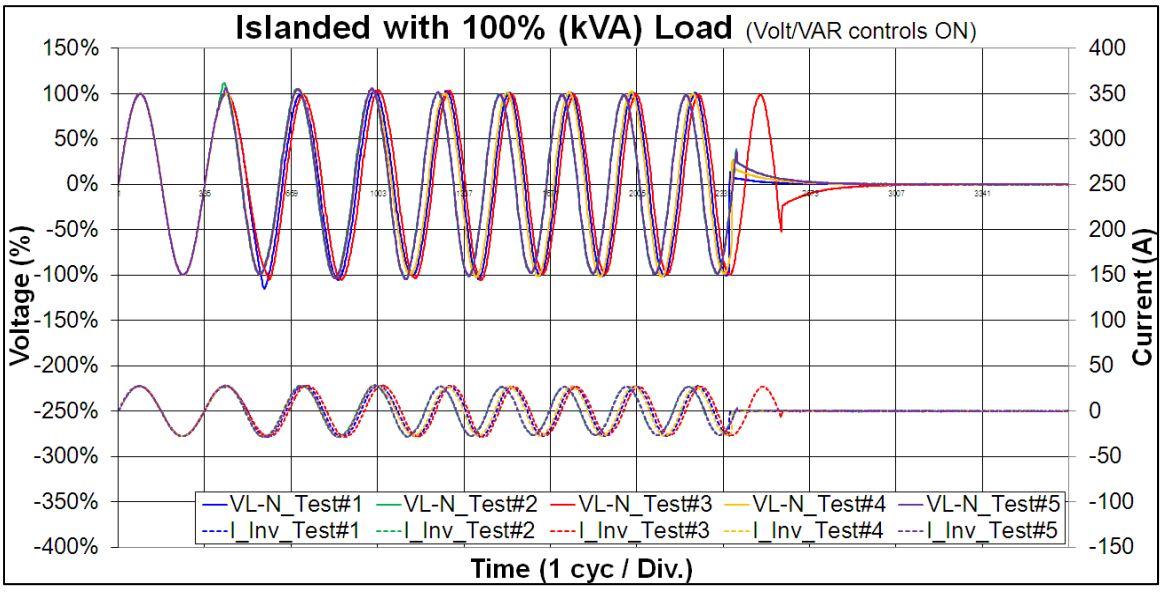

Figure 15.2.1 Inverter Disconnected with Volt/VAR

Island Settings #2:

- Enabled inverter volt/var control features
- Real and reactive load reasonably matched inverter generation
- Disabled the inverters anti-islanding detection setting (“Escalation factor”)
- Under-frequency protection was set low (< 50 Hz)

Test Results #2: are shown in Figure 15.2.2

- Even with similar protection settings as Section 15.1, the inverter still trips off relatively quickly
- Voltages fluctuate as high as 113% nominal voltage
- Inverter shuts down within 6 cycles after being disconnected

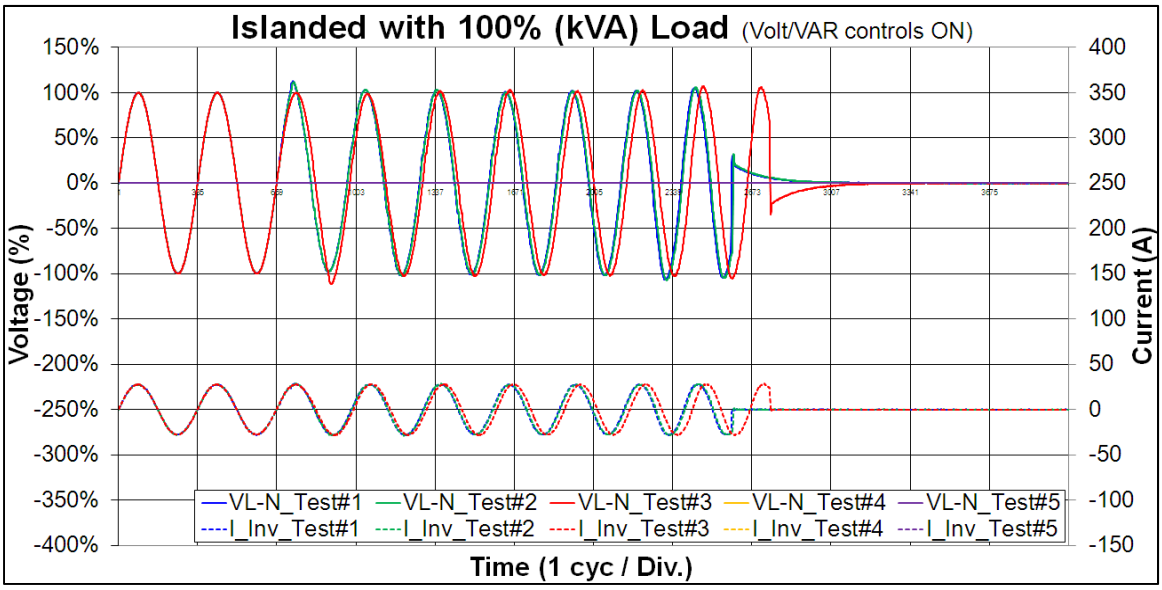

Figure 15.2.2 Inverter Disconnected with Volt/VAR and Disabled Protection

15.3 Islanding Potential during Voltage Ride Through

Another concern regarding advanced features is effects of volt/var controls when disconnecting from the grid during low voltage conditions. Hence the inverter was disconnected from the grid with matched load during the low voltage region of a fault induced delayed voltage recovery (FIDVR) profile. The tests revealed no evidence that the inverters volt/var features will compromise anti-islanding protection during a low voltage ride through event.

Island Settings:

- Enabled inverter volt/var control features
- Real and reactive load reasonably matched inverter generation

Test Results: as shown in Figure 15.3.1

- Before grid disconnection, the inverter begins riding through the low voltage event
  - Current increases to its maximum value to power generation
  - Real power is still being generated at a reduced output
  - Reactive power is increased to its maximum output per the Volt/VAR support features
- When the inverter was physically disconnected from the grid by a circuit breaker, the inverter almost immediately shuts down
  - Inverter current, real, and reactive power begin decreasing within several cycles
  - Inverter voltage appears to increase from 58% to 104% nominal voltage before shutdown

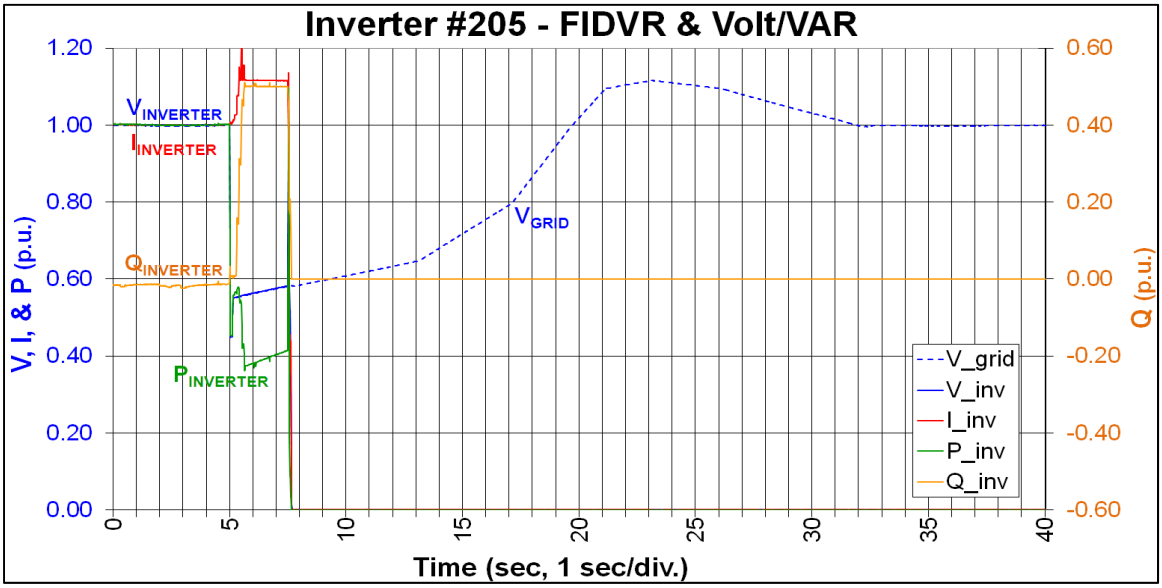

Figure 15.3.1 Inverter with Volt/VAR Disconnected during LVRT

16.0 ISLANDING POTENTIAL (PARALLELED INVERTERS)

With multiple residential inverters on a circuit, there is a concern that these paralleled inverters anti-islanding protection may interfere with each other. Utilities that have this concern want to ensure the safety of field personnel by preventing self-sustaining islands from occurring on the grid. The following test results are for Inverters 201, 202, 203, and 205 in parallel.

16.1 Islanding Potential with Adjusted Protection Settings

The inverters have a remote possibility of being islanded if someone were to enter the wrong protection settings for these devices. All of the following settings must be changed in order for the inverters to remain generating power: wider frequency protection beyond IEEE 1547, match load and generation, and anti-islanding protection disabled. The inverters were islanded indefinitely and 1 hour of data was captured during the islanding condition.

Island Settings #1:

- Disabled the inverters anti-islanding protection setting (“Escalation factor”)
- Real and reactive load reasonably matched total inverter generation
- Under-frequency protection was set low (< 50 Hz)
- Disabled Inverter 205 volt/var control features

Test Results #1: are shown in Figure 16.1.1

- Inverter begins operating at approximately 58.5 Hz while successfully islanded
  - U.S. frequency protection standards may result in the inverter tripping
- A static PF of 0.9 leading for all inverters was used to maintain consistent generation values

- With constant load, inverter remains islanded for over an hour

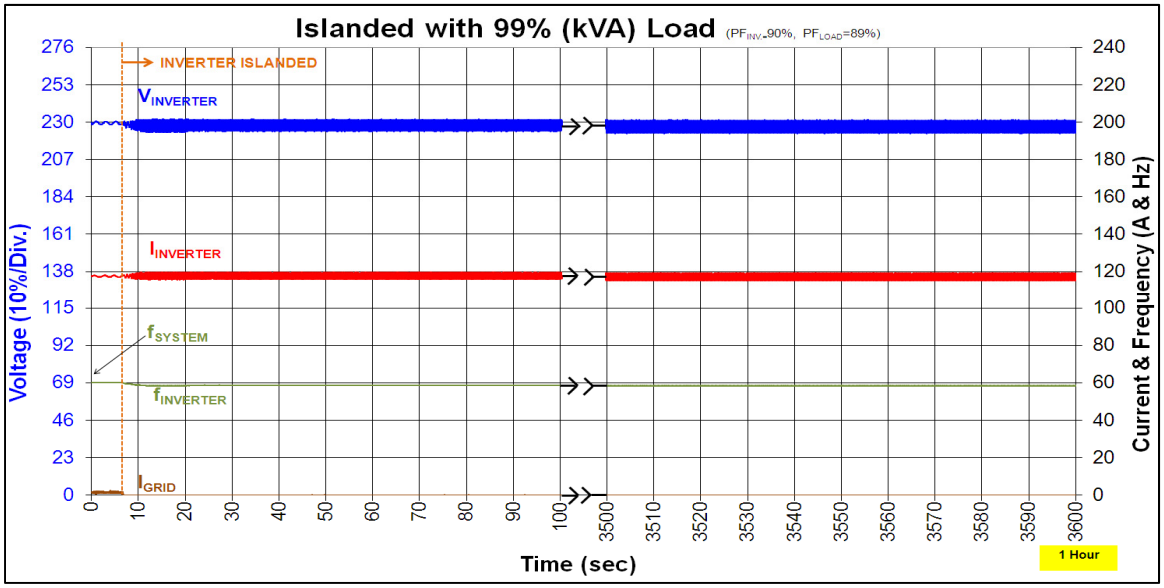

Figure 16.1.1 Inverters Islanded with Static Power Factors

Island Settings #2:

- Disabled the inverters anti-islanding detection setting (“Escalation factor”)
- Real and reactive load reasonably matched total inverter generation
- Under-frequency protection was set low (< 50 Hz)
- Enabled Inverter 205 volt/var control features

Test Results #2: are shown in Figure 16.1.2

- Inverter begins operating at approximately 58.8 Hz while successfully islanded
  - U.S. frequency protection standards may result in the inverter tripping
- A static PF of 0.9 leading for Inverters 201, 202, and 203 was used to maintain consistent generation values with flexibility from Inverter 205’s volt/var controls
- With constant load, inverter remains islanded for over an hour

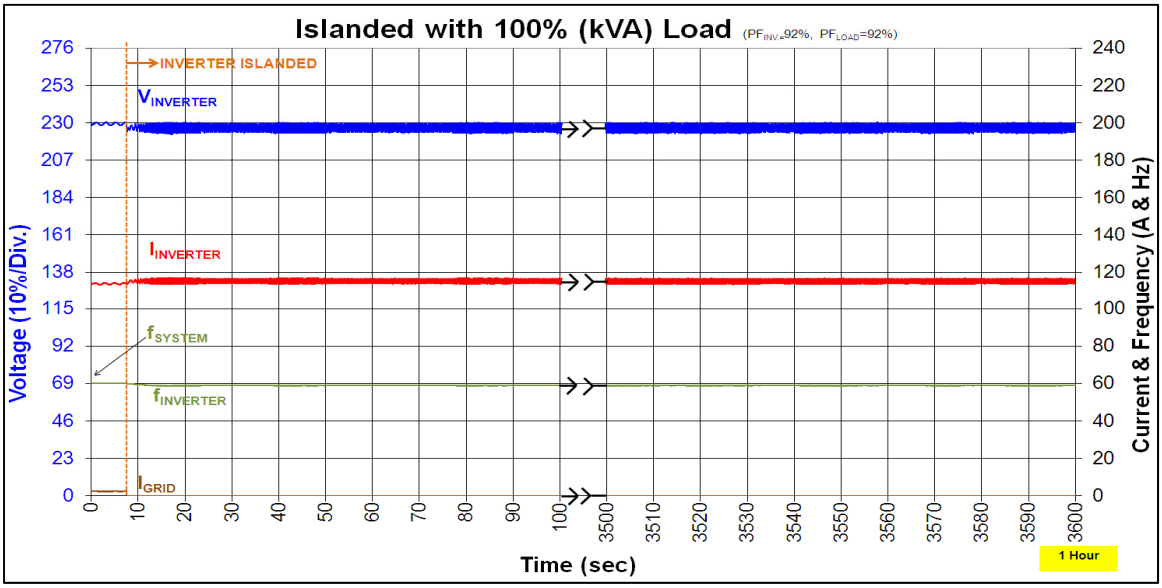

Figure 16.1.2 Inverters Islanded with Static Power Factors and Volt/VAR Controls

16.2 Islanding Potential during Voltage Ride Through

Another concern regarding multiple inverters is effects of their anti-islanding controls when disconnecting from the grid during low voltage conditions. Hence the inverters were disconnected from the grid with matched load during the low voltage region of a fault induced delayed voltage recovery (FIDVR) profile. The tests revealed no evidence that the anti-islanding protection will be compromised during a low voltage ride through event.

Island Settings:

- Disabled Inverter 205 volt/var control features
- Real and reactive load reasonably matched inverter generation

Test Results: are shown in Figure 16.2.1

- Before grid disconnection, the inverter begins riding through the low voltage event
  - Current increases to its maximum value to power generation
  - Real and reactive power is still being generated at a reduced output
- When the inverter was physically disconnected from the grid by a circuit breaker, the inverter almost immediately shuts down
  - Inverter current, real, and reactive power begin decreasing within several cycles
  - Inverter voltage appears to increase from 56% to 106% nominal voltage before shutdown

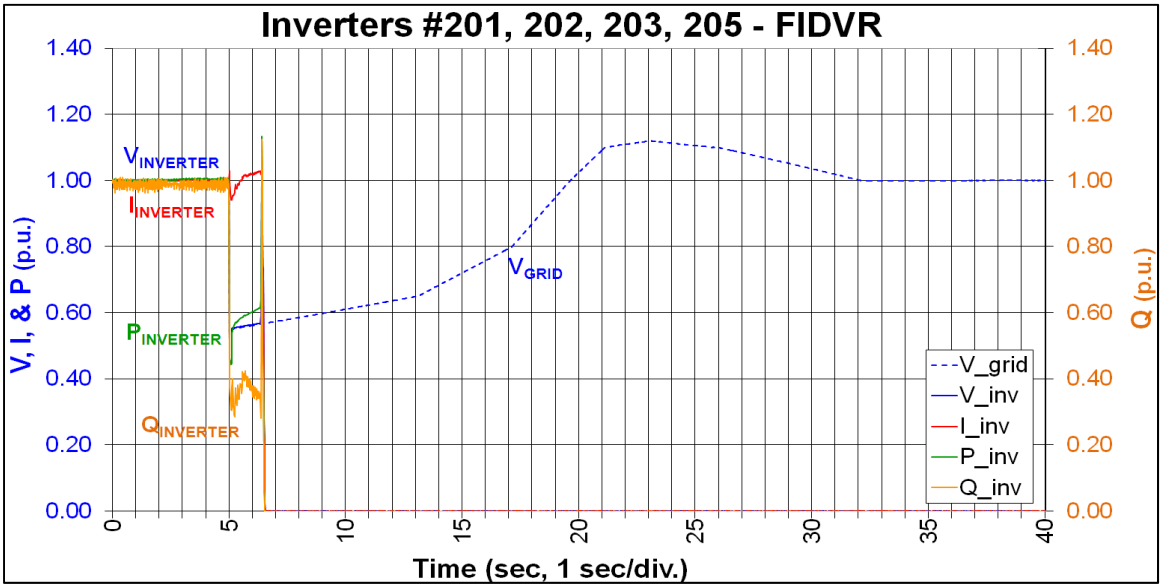

Figure 16.2.1 Paralleled Inverters Disconnected during LVRT